

SHEET

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SHEET

TITLE

32	RT8120_PCH
33	DISCRETE POWER1
34	NCT3933
35	ATX POWER , A_-PROCHOT
36	KB_MS_USB
37	OC BUTTON
38	F_USB30
39	F_USB20
40	R_USB30
41	Realtek ALC1150
42	REAR AUDIO JACK
43	Audio Power
44	ASM1142 USB31A
45	DUAL LAN-B~I219
46	DUAL LAN-C~I211
47	DUAL USB30_LAN-I219_I211
48	Etron EJ179V_A SW&CC
49	IDT6V41510_20_CLK BUFFER
50	COM , LPT , TPM , THB
51	F_PANEL
52	ASM1061
53	DVI CONN
54	HDMI 20 MCDP2800-BA
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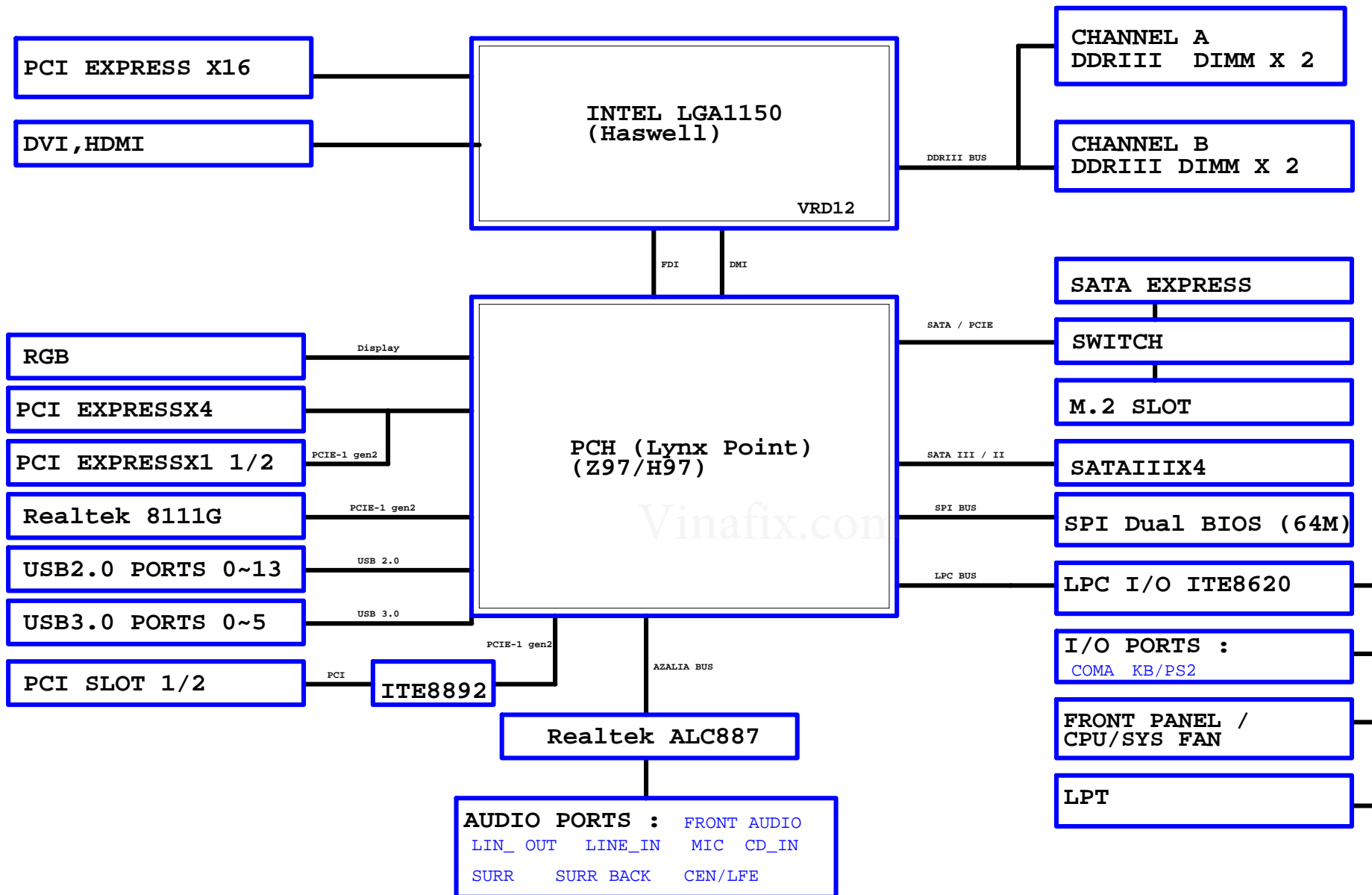
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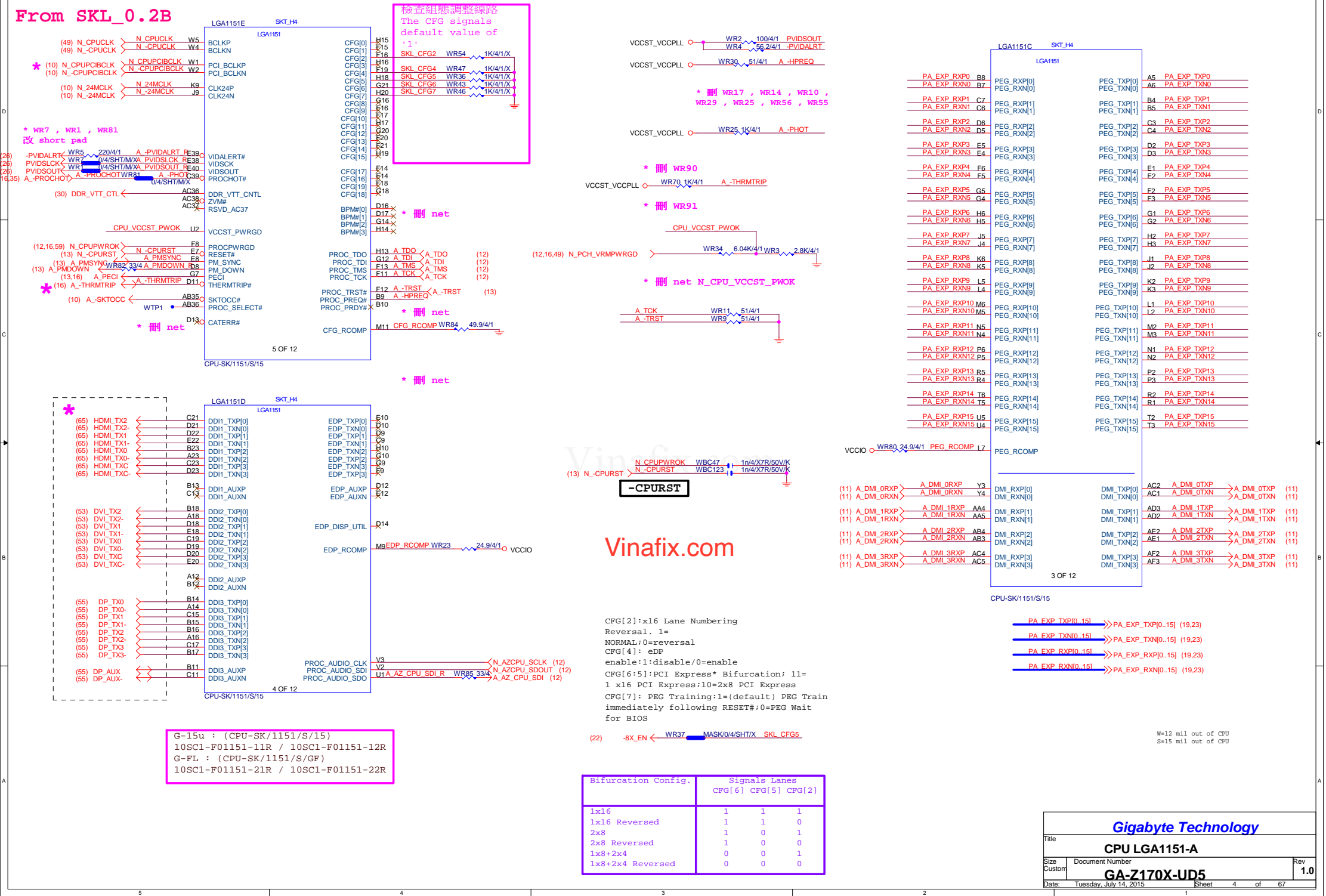
Circuit or PCB layout change

DATE	Change Item	Reason
2014/11/28 PCB:0.1	1.PCB first release 2.線路由GA-Z1704-SLI-01-1128B.DSN來修改	
2015/01/26 PCB:0.2	1. Update TYPEC footprint "USB-TYPEC-1" 2. 增加IDT6V41510/IDT6V41520 co-lay 線路 、增加co-lay 電阻 table 、原CKR16改接CKU1 PIN 16 3. 測試點位置偏移M2 CLK 4. DDRVTT ADD DAR110,DAR111 5. OC,ECO BUTTON change footprint 6. Add NXP TO VGA CLK COST DOWN	
2015/01/29 PCB:0.1	1. AUDIO CHANGE TO ALC1150 2. LAN CHANGE TO INTEL I211AT 3. ADD USB 3.1 ASM1142 4. DELETE DP-VGA 5. DELETE GL850S 6. ADD SYS_FAN4 7. DELETE USB DAC POWER 8. Modify from Z1704X-GAMING 7-02A.DSN 9. PCIE_X4_N_GPP_E3 CHANGE TO N_GPP_E4	GA-Z170X-UD5 Rev 0.1
2015/05/28 PCB:0.2	1.42B&60B&80B文字改為42D&60D&80D 2.VCORE_VS移到CPU下方 3.PCIE_X4改為PCIE_SLOT-64STH-1 4.NX1請導入最新LAYOUT RULE 5.文字改SATA 3 6/7 6. Add VD1 7. Add THD3 8. TCAQ3 改為TCAQ1&TCAQ2 9. 刪除WR100,WR101,NR300,NR301,NR302NR303,WR102,WR103 10.U6 rename to DB_PORT 11. Audio update a. CR44 update footprint "R0603-RH-SHORT30-MASK" b. MOATRL1/2/3/4 update footprint "R0402-2-SHORT20-MASK"	GA-Z170X-UD5 Rev 0.2
2015/06/03 PCB:0.3	1.由Z170X-UD5 REV 0.2來修改 2.修改PCIE_X4 跟M2A切換線路 3.Net N_GPP_G4改為N_GPP_D16 4. TYPEC 改TI SOLUTION 5. Add HDMI level shift	GA-Z170X-UD5 Rev 0.3
2015/06/26	由Z170X-UD5 Rev 0.3來修改 1.Add SWPR4, SWPD1 可放在NR270旁邊 2.all 0ohm改short pad 3.WR94改為0 ohm 4.Add MA_DR9 close to MA_DQ3 5.DDR Power右移&下移 6.Add NPC10 close to CPU	GA-Z170X-UD5 Rev 9.0
2015/07/03	1. BIOS_PH改Mask 2. SWPU2 Net改PCIE_X4_M2S 3. 增加THR19不上件 (以色列LOGO測試反應問題後，INTEL建議) 4. Add DFR4 5. Add MAC10	GA-Z170X-UD5 Rev 9.0

BLOCK DIAGRAM



From SKL_0.2B



G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R

Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0

Gigabyte Technology

CPU LGA1151-A

Size Custom

Document Number

GA-2170X-UD5

Date: Tuesday, July 14, 2015

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Rev 1.0

* 改DDR4 net

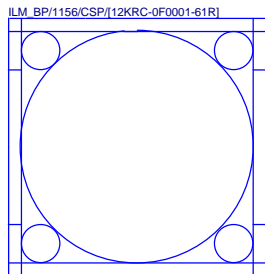
LGA1151A SKT_H4 LGA1151			
MDA0 AE38	DDR0_DQ[0]	DDR0_CK[0]	AW18 M_DCLKA0 <=> M_DCLKA0 (8)
MDA1 AE37	DDR0_DQ[1]	DDR0_CK[1]	AW18 M_DCLKA0 <=> M_DCLKA0 (8)
MDA2 AG38	DDR0_DQ[2]	DDR0_CK[1]	AW17 M_DCLKA1 <=> M_DCLKA1 (8)
MDA3 AG37	DDR0_DQ[3]	DDR0_CK[1]	AW17 M_DCLKA1 <=> M_DCLKA1 (8)
MDA4 AE38	DDR0_DQ[4]	DDR0_CK[2]	AW16 M_DCLKA2 <=> M_DCLKA2 (8)
MDA5 AE40	DDR0_DQ[5]	DDR0_CK[2]	AW16 M_DCLKA2 <=> M_DCLKA2 (8)
MDA6 AG38	DDR0_DQ[6]	DDR0_CK[3]	AT18 M_DCLKA3 <=> M_DCLKA3 (8)
MDA7 AG40	DDR0_DQ[7]	DDR0_CK[3]	AT18 M_DCLKA3 <=> M_DCLKA3 (8)
MDA8 AJ38	DDR0_DQ[8]		AW16 M_DCLKA3 <=> M_DCLKA3 (8)
MDA9 AJ37	DDR0_DQ[9]		AY24 CKEA0 <=> CKEA0 (8)
MDA10 AL38	DDR0_DQ[10]	DDR0_CKE[0]	AY24 CKEA1 <=> CKEA1 (8)
MDA11 AL37	DDR0_DQ[11]	DDR0_CKE[1]	AY24 CKEA2 <=> CKEA2 (8)
MDA12 AL40	DDR0_DQ[12]	DDR0_CKE[2]	AY25 CKEA3 <=> CKEA3 (8)
MDA13 AL39	DDR0_DQ[13]		
MDA14 AL39	DDR0_DQ[14]	DDR0_CS[0]	AW12 M_CSA0 <=> M_CSA0 (8)
MDA15 AL40	DDR0_DQ[15]	DDR0_CS[1]	AW12 M_CSA1 <=> M_CSA1 (8)
MDA16 AX38	DDR0_DQ[16]	DDR0_CS[2]	AW13 M_CSA2 <=> M_CSA2 (8)
MDA17 AX40	DDR0_DQ[17]	DDR0_CS[2]	AW10 M_CSA3 <=> M_CSA3 (8)
MDA18 AR38	DDR0_DQ[18]	DDR0_CS[3]	
MDA19 AR37	DDR0_DQ[19]	DDR0_ODT[0]	AW11 M_ODT_A0
MDA20 AN39	DDR0_DQ[20]	DDR0_ODT[1]	AW14 M_ODT_A1
MDA21 AN37	DDR0_DQ[21]	DDR0_ODT[2]	AW12 M_ODT_A2
MDA22 AR39	DDR0_DQ[22]	DDR0_ODT[3]	AY10 M_ODT_A3
MDA23 AR40	DDR0_DQ[23]		
MDA24 AW37	DDR0_DQ[24]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AY13 SBAA0 <=> SBAA0 (8)
MDA25 AL38	DDR0_DQ[25]	DDR0_BA[1]/DDR0_CAB[5]/DDR0_BA[1]	AY15 SBAA1 <=> SBAA1 (8)
MDA26 AV35	DDR0_DQ[26]	DDR0_BA[2]/DDR0_CAB[5]/DDR0_BG[0]	AW23 BG_A0 <=> BG_A0 (8)
MDA27 AW36	DDR0_DQ[27]		
MDA28 AL37	DDR0_DQ[28]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AW13 MAAA16
MDA29 AV37	DDR0_DQ[29]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AW14 MAAA14
MDA30 AT36	DDR0_DQ[30]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AW11 MAAA15
MDA31 AU38	DDR0_DQ[31]		
MDA32 AX38	DDR0_DQ[32]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AW15 MAAA0
MDA33 AW38	DDR0_DQ[33]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	AW18 MAAA1
MDA34 AV6	DDR0_DQ[34]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AW17 MAAA2
MDA35 AU6	DDR0_DQ[35]	DDR0_MA[3]	AW19 MAAA3
MDA36 AU8	DDR0_DQ[36]	DDR0_MA[4]	AT19 MAAA4
MDA37 AV8	DDR0_DQ[37]	DDR0_MA[5]	AW20 MAAA5
MDA38 AW6	DDR0_DQ[38]	DDR0_MA[6]	AW21 MAAA7
MDA39 AV6	DDR0_DQ[39]	DDR0_MA[7]	AT20 MAAA8
MDA40 AY4	DDR0_DQ[40]	DDR0_MA[8]	AT22 MAAA9
MDA41 AV4	DDR0_DQ[41]	DDR0_MA[9]	AW22 MAAA11
MDA42 AT2	DDR0_DQ[42]	DDR0_MA[10]	AW22 MAAA12
MDA43 AT2	DDR0_DQ[43]	DDR0_MA[11]	AW22 MAAA13
MDA44 AV3	DDR0_DQ[44]	DDR0_MA[12]	AW23 BG_A1 <=> BG_A1 (8)
MDA45 AW4	DDR0_DQ[45]	DDR0_MA[13]	AW24 M_ACT_A <=> M_ACT_A (8)
MDA46 AT4	DDR0_DQ[46]	DDR0_MA[14]	
MDA47 AT3	DDR0_DQ[47]	DDR0_MA[15]	
MDA48 AP2	DDR0_DQ[48]		
MDA49 AM4	DDR0_DQ[49]	DDR0_PAR	AY15 <=> M_DDR_PARA (8)
MDA50 AP3	DDR0_DQ[50]	DDR0_ALERT#	AT23 <=> M_ALERT_A (8)
MDA51 AM3	DDR0_DQ[51]		
MDA52 AP4	DDR0_DQ[52]	DDR0_DQS[0]	AF39 M_DQSA0
MDA53 AM2	DDR0_DQ[53]	DDR0_DQS[1]	AK39 M_DQSA2
MDA54 AP1	DDR0_DQ[54]	DDR0_DQS[2]	AP39 M_DQSA2
MDA55 AM1	DDR0_DQ[55]	DDR0_DQS[3]	AW36 M_DQSA3
MDA56 AK3	DDR0_DQ[56]	DDR0_DQS[4]	AW7 M_DQSA5
MDA57 AH1	DDR0_DQ[57]	DDR0_DQS[5]	AJ3 M_DQSA6
MDA58 AK4	DDR0_DQ[58]	DDR0_DQS[6]	AJ3 M_DQSA7
MDA59 AH2	DDR0_DQ[59]	DDR0_DQS[7]	
MDA60 AH4	DDR0_DQ[60]		
MDA61 AK2	DDR0_DQ[61]	DDR0_DQSP[0]	AF38 M_DQSA0
MDA62 AH3	DDR0_DQ[62]	DDR0_DQSP[1]	AK38 M_DQSA1
MDA63 AK1	DDR0_DQ[63]	DDR0_DQSP[2]	AP38 M_DQSA2
		DDR0_DQSP[3]	AW36 M_DQSA3
		DDR0_DQSP[4]	AW7 M_DQSA5
		DDR0_DQSP[5]	AJ3 M_DQSA6
		DDR0_DQSP[6]	AJ2 M_DQSA7
		DDR0_DQSP[7]	
		DDR0_DQSP[8]	AF32
		DDR0_DQSP[9]	AJ32

DDR CHANNEL A

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CPU-SK/1151/S/15

LGA1151



Need check the new CPU MB

LGA1151B SKT_H4 LGA1151			
MDB0 AD34	DDR1_DQ[0]/DDR0_DQ[16]	DDR1_CK[0]	AM20 M_DCLKB0 <=> M_DCLKB0 (9)
MDB1 AD35	DDR1_DQ[1]/DDR0_DQ[17]	DDR1_CK[1]	AM21 M_DCLKB0 <=> M_DCLKB0 (9)
MDB2 AG35	DDR1_DQ[2]/DDR0_DQ[18]	DDR1_CK[2]	AP22 M_DCLKB1 <=> M_DCLKB1 (9)
MDB3 AH35	DDR1_DQ[3]/DDR0_DQ[19]	DDR1_CK[1]	AP21 M_DCLKB1 <=> M_DCLKB1 (9)
MDB4 AE35	DDR1_DQ[4]/DDR0_DQ[20]	DDR1_CK[2]	AN20 M_DCLKB2 <=> M_DCLKB2 (9)
MDB5 AE34	DDR1_DQ[5]/DDR0_DQ[21]	DDR1_CK[2]	AN21 M_DCLKB2 <=> M_DCLKB2 (9)
MDB6 AG34	DDR1_DQ[6]/DDR0_DQ[22]	DDR1_CK[3]	AP19 M_DCLKB3 <=> M_DCLKB3 (9)
MDB7 AH34	DDR1_DQ[7]/DDR0_DQ[23]	DDR1_CK[3]	AP20 M_DCLKB3 <=> M_DCLKB3 (9)
MDB8 AK35	DDR1_DQ[8]/DDR0_DQ[24]		
MDB9 AL35	DDR1_DQ[9]/DDR0_DQ[25]	DDR1_CKE[0]	AY29 CKEB0 <=> CKEB0 (9)
MDB10 AL32	DDR1_DQ[10]/DDR0_DQ[26]	DDR1_CKE[1]	AY29 CKEB1 <=> CKEB1 (9)
MDB11 AL32	DDR1_DQ[11]/DDR0_DQ[27]	DDR1_CKE[2]	AY29 CKEB2 <=> CKEB2 (9)
MDB12 AK34	DDR1_DQ[12]/DDR0_DQ[28]	DDR1_CKE[3]	AY29 CKEB3 <=> CKEB3 (9)
MDB13 AL34	DDR1_DQ[13]/DDR0_DQ[29]		
MDB14 AK31	DDR1_DQ[14]/DDR0_DQ[30]	DDR1_CS[0]	AP17 M_CSB0 <=> M_CSB0 (9)
MDB15 AL31	DDR1_DQ[15]/DDR0_DQ[31]	DDR1_CS[1]	AN15 M_CSB1 <=> M_CSB1 (9)
MDB16 AP35	DDR1_DQ[16]/DDR0_DQ[32]	DDR1_CS[2]	AM15 M_CSB2 <=> M_CSB2 (9)
MDB17 AN35	DDR1_DQ[17]/DDR0_DQ[33]	DDR1_CS[3]	AM15 M_CSB3 <=> M_CSB3 (9)
MDB18 AN32	DDR1_DQ[18]/DDR0_DQ[34]		
MDB19 AP32	DDR1_DQ[19]/DDR0_DQ[35]	DDR1_ODT[0]	AM16 M_ODT_B0
MDB20 AN34	DDR1_DQ[20]/DDR0_DQ[36]	DDR1_ODT[1]	AL16 M_ODT_B1
MDB21 AP34	DDR1_DQ[21]/DDR0_DQ[37]	DDR1_ODT[2]	AL17 M_ODT_B2
MDB22 AN31	DDR1_DQ[22]/DDR0_DQ[38]	DDR1_ODT[3]	AL15 M_ODT_B3
MDB23 AP31	DDR1_DQ[23]/DDR0_DQ[39]		
MDB24 AL29	DDR1_DQ[24]/DDR0_DQ[40]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AN18 MAA16
MDB25 AM29	DDR1_DQ[25]/DDR0_DQ[41]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AL17 MAA17
MDB26 AP29	DDR1_DQ[26]/DDR0_DQ[42]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AL16 MAA15
MDB27 AR29	DDR1_DQ[27]/DDR0_DQ[43]		
MDB28 AM28	DDR1_DQ[28]/DDR0_DQ[44]	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	AL18 SBAB0 <=> SBAB0 (9)
MDB29 AL28	DDR1_DQ[29]/DDR0_DQ[45]	DDR1_BA[1]/DDR1_CAB[5]/DDR1_BA[1]	AM18 SBAB1 <=> SBAB1 (9)
MDB30 AR28	DDR1_DQ[30]/DDR0_DQ[46]	DDR1_BA[2]/DDR1_CAB[5]/DDR1_BG[0]	AW28 BG_B0 <=> BG_B0 (9)
MDB31 AR28	DDR1_DQ[31]/DDR0_DQ[47]		
MDB32 AR12	DDR1_DQ[32]/DDR0_DQ[48]		
MDB33 AP12	DDR1_DQ[33]/DDR0_DQ[49]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	AL19 MAA19
MDB34 AM13	DDR1_DQ[34]/DDR0_DQ[50]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AL22 MAA18
MDB35 AL13	DDR1_DQ[35]/DDR0_DQ[51]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AM22 MAA12
MDB36 AR13	DDR1_DQ[36]/DDR0_DQ[52]	DDR1_MA[3]	AM23 MAA13
MDB37 AP13	DDR1_DQ[37]/DDR0_DQ[53]	DDR1_MA[4]	AP23 MAA14
MDB38 AM12	DDR1_DQ[38]/DDR0_DQ[54]	DDR1_MA[5]	AP23 MAA15
MDB39 AL12	DDR1_DQ[39]/DDR0_DQ[55]	DDR1_MA[6]	AW26 MAA16
MDB40 AP10	DDR1_DQ[40]/DDR0_DQ[56]	DDR1_MA[7]	AY26 MAA17
MDB41 AR10	DDR1_DQ[41]/DDR0_DQ[57]	DDR1_MA[8]	AW27 MAA18
MDB42 AR7	DDR1_DQ[42]/DDR0_DQ[58]	DDR1_MA[9]	AW27 MAA19
MDB43 AF7	DDR1_DQ[43]/DDR0_DQ[59]	DDR1_MA[10]	AJ27 MAA11
MDB44 AR9	DDR1_DQ[44]/DDR0_DQ[60]	DDR1_MA[11]	AJ27 MAA12
MDB45 AP9	DDR1_DQ[45]/DDR0_DQ[61]	DDR1_MA[12]	AV25 MAA13
MDB46 AR6	DDR1_DQ[46]/DDR0_DQ[62]	DDR1_MA[13]	AY18 MAA13
MDB47 AP6	DDR1_DQ[47]/DDR0_DQ[63]	DDR1_MA[14]	AY28 BG_B1 <=> BG_B1 (9)
MDB48 AM10	DDR1_DQ[48]	DDR1_MA[15]	AJ28 M_ACT_B <=> M_ACT_B (9)
MDB49 AL10	DDR1_DQ[49]		
MDB50 AM7	DDR1_DQ[50]	DDR1_PAR	AL20 <=> M_DDR_PARB (9)
MDB51 AL7	DDR1_DQ[51]	DDR1_ALERT#	AY25 <=> M_ALERT_B (9)
MDB52 AM8	DDR1_DQ[52]		
MDB53 AL9	DDR1_DQ[53]	DDR1_DQS[0]	AF34 M_DQSB0
MDB54 AM6	DDR1_DQ[54]	DDR1_DQS[1]	AK33 M_DQSB1
MDB55 AL6	DDR1_DQ[55]	DDR1_DQS[2]	AN33 M_DQSB2
MDB56 AJ6	DDR1_DQ[56]	DDR1_DQS[3]	AN29 M_DQSB3
MDB57 AJ7	DDR1_DQ[57]	DDR1_DQS[4]	AN13 M_DQSB4
MDB58 AF6	DDR1_DQ[58]	DDR1_DQS[5]	AM8 M_DQSB5
MDB59 AF7	DDR1_DQ[59]	DDR1_DQS[6]	AG6 M_DQSB7
MDB60 AH7	DDR1_DQ[60]	DDR1_DQS[7]	
MDB61 AH6	DDR1_DQ[61]		
MDB62 AF7	DDR1_DQ[62]	DDR1_DQSP[0]	AF35 M_DQSB0
MDB63 AF6	DDR1_DQ[63]	DDR1_DQSP[1]	AL33 M_DQSB1
		DDR1_DQSP[2]	AN28 M_DQSB2
		DDR1_DQSP[3]	AN23 M_DQSB3
		DDR1_DQSP[4]	AN12 M_DQSB4
		DDR1_DQSP[5]	AP8 M_DQSB5
		DDR1_DQSP[6]	AL8 M_DQSB6
		DDR1_DQSP[7]	AG7 M_DQSB7
		DDR1_DQSP[8]	AN25
		DDR1_DQSP[9]	AN26

DDR CHANNEL B

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- (8) MODT_A[0..3] <=> MODT_A0..31
- (9) MODT_B[0..3] <=> MODT_B0..31
- (8) MDA[0..63] <=> MDA0..631
- (9) MDB[0..63] <=> MDB0..631
- (8) M_DQSA[0..7] <=> M_DQSA0..71
- (8) M_DQSB[0..7] <=> M_DQSB0..71
- (8) MAA[0..16] <=> MAA0..161
- (9) MAA[0..16] <=> MAA0..161
- (9) M_DQSB[0..7] <=> M_DQSB0..71
- (9) M_DQSB[0..7] <=> M_DQSB0..71

Gigabyte Technology

Title

CPU LGA1151-B

Size

Document Number

GA-Z170X-UD5

Rev

1.0

Date:

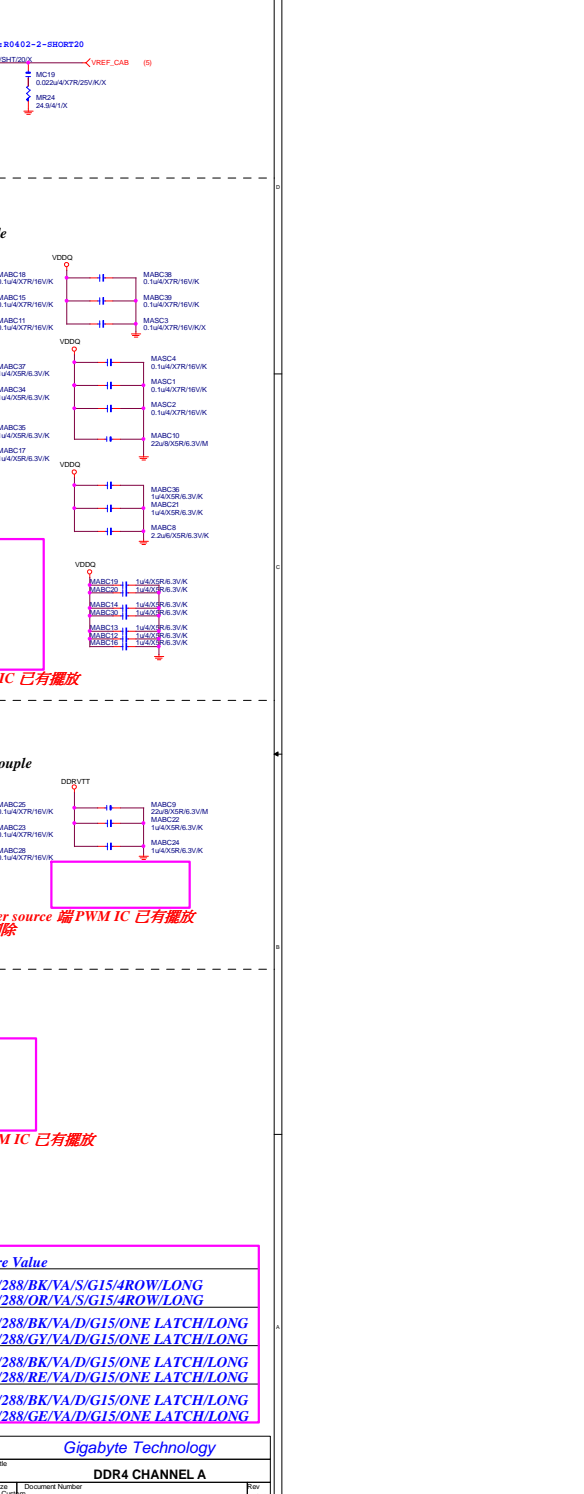
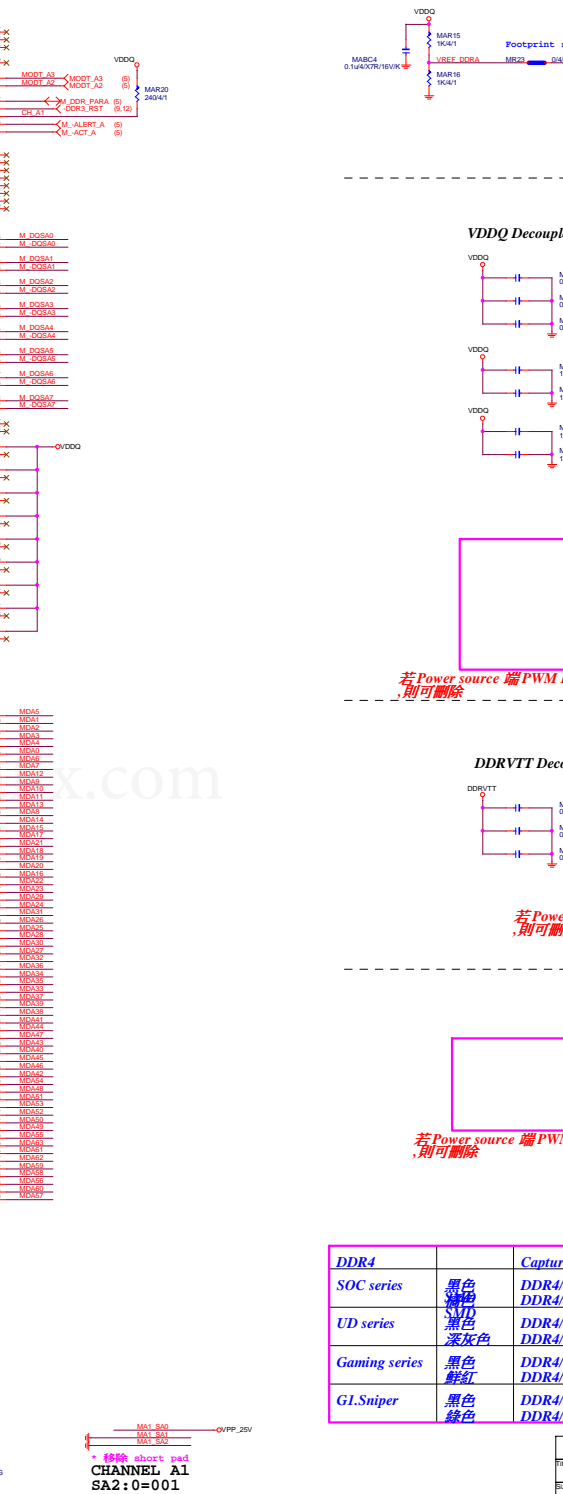
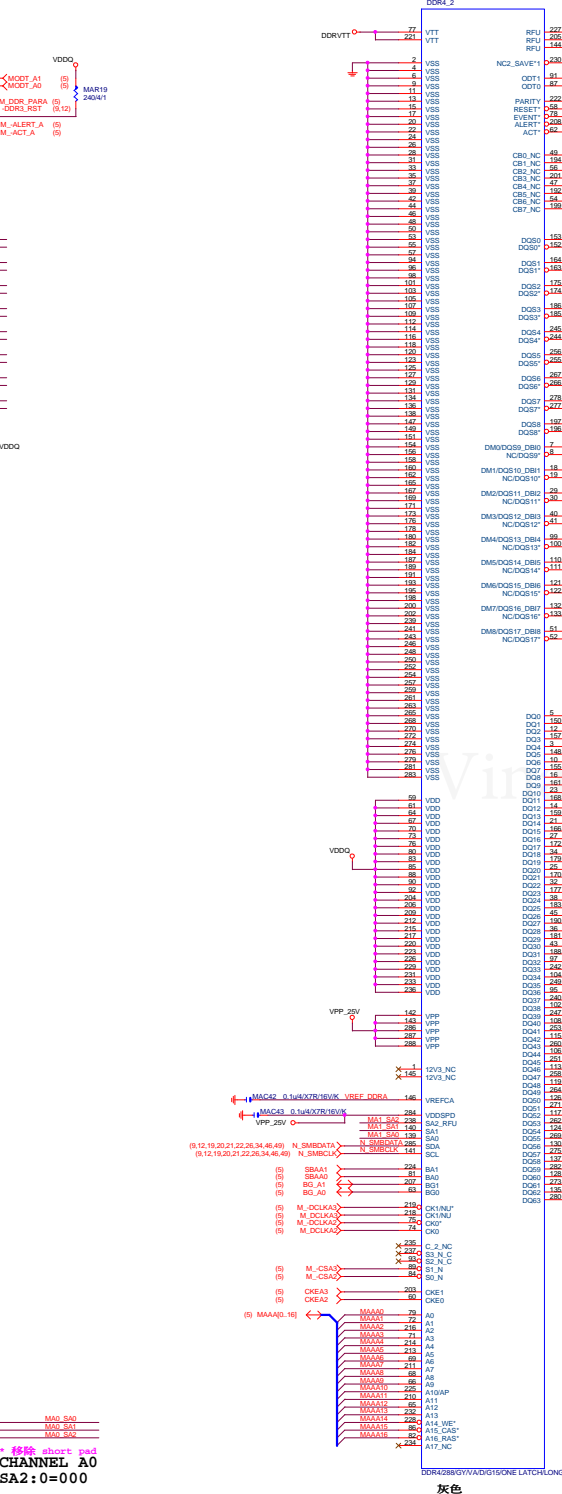
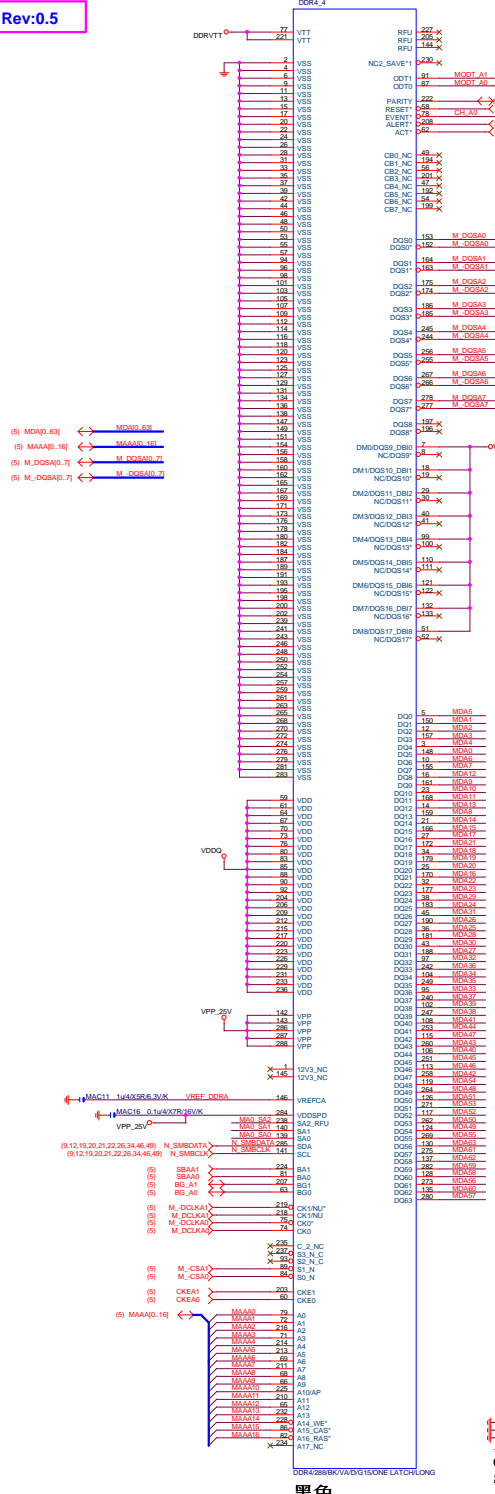
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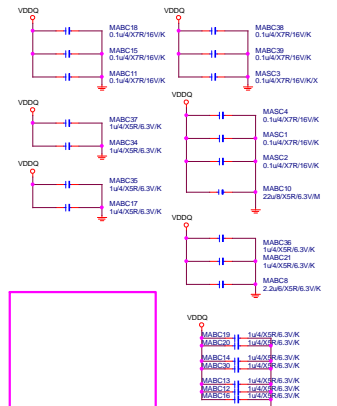
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of

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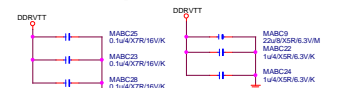


VDDQ Decouple



若Power source 端PWM IC 已有擺放, 則可刪除

DDRVTT Decouple



若Power source 端PWM IC 已有擺放, 則可刪除

DDRVTT Decouple



若Power source 端PWM IC 已有擺放, 則可刪除

DDR4	Capture Value
SOC series	DDR4/288/BK/VA/S/G15/4ROW/LONG DDR4/288/OR/VA/S/G15/4ROW/LONG
UD series	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG DDR4/288/GY/VA/D/G15/ONE LATCH/LONG
Gaming series	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG DDR4/288/RE/VA/D/G15/ONE LATCH/LONG
GI.Sniper	DDR4/288/BK/VA/D/G15/ONE LATCH/LONG DDR4/288/GE/VA/D/G15/ONE LATCH/LONG

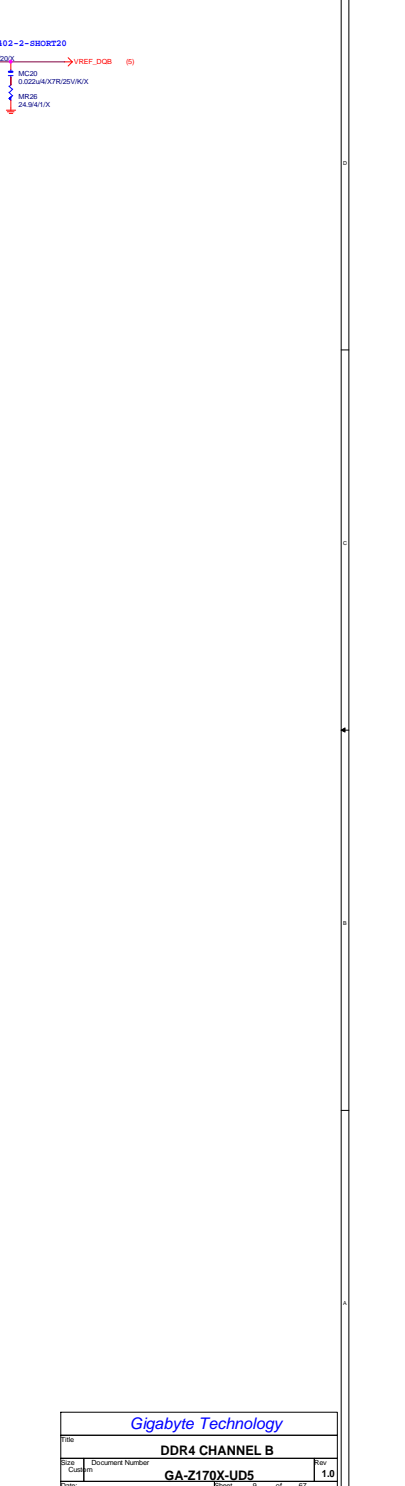
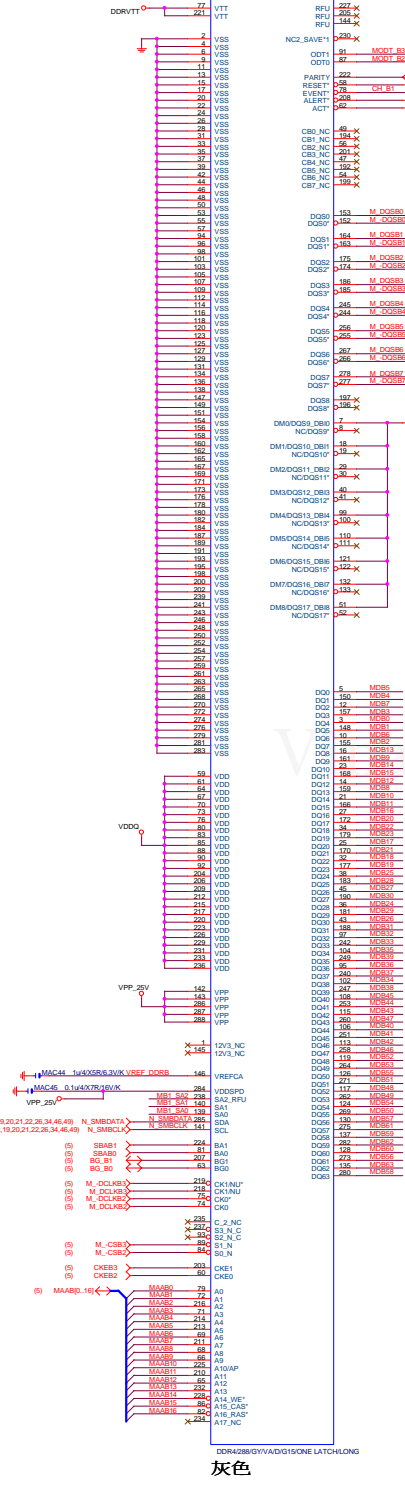
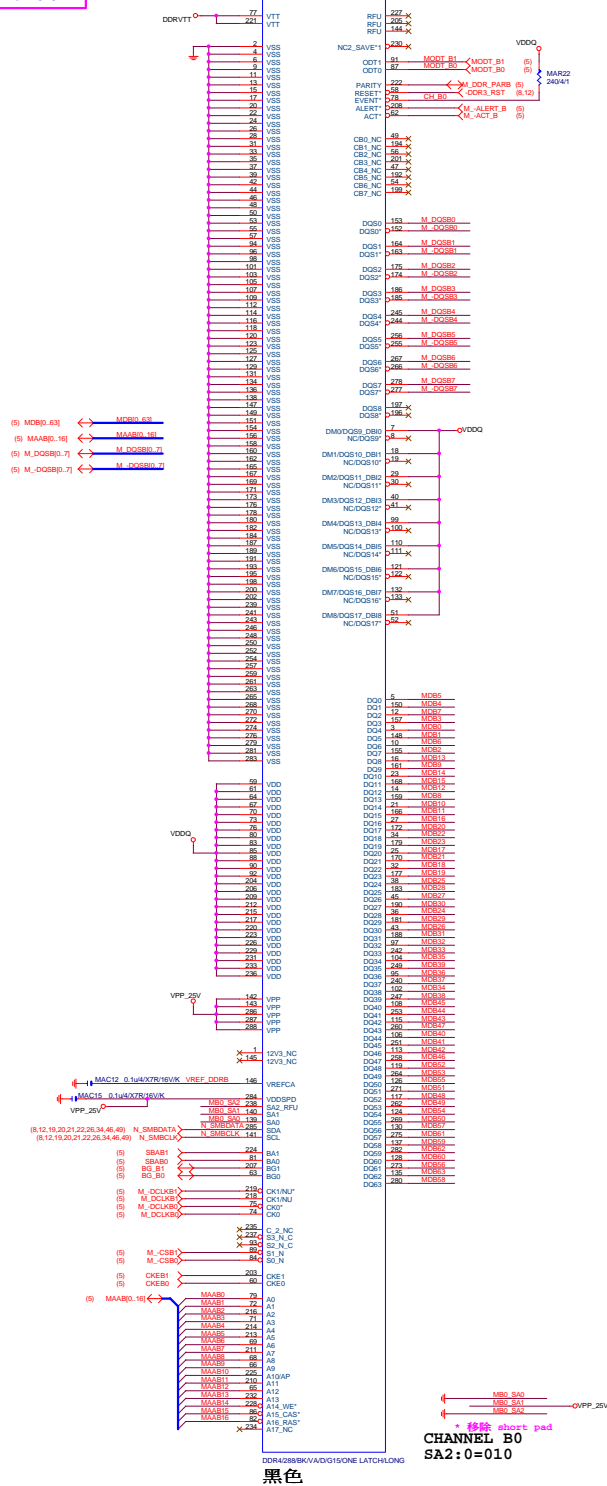
Gigabyte Technology

File: DDR4 CHANNEL A

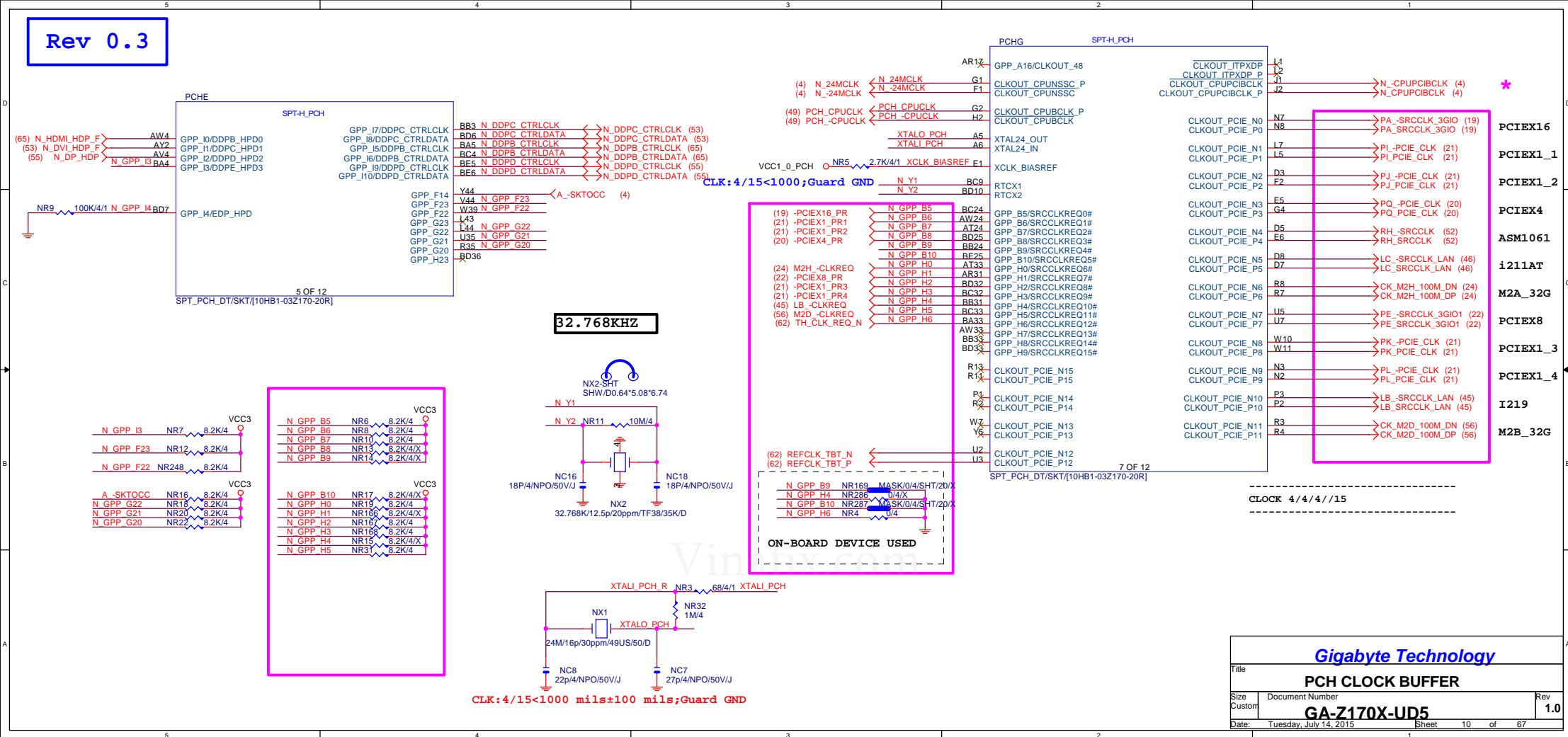
Size: Document Number

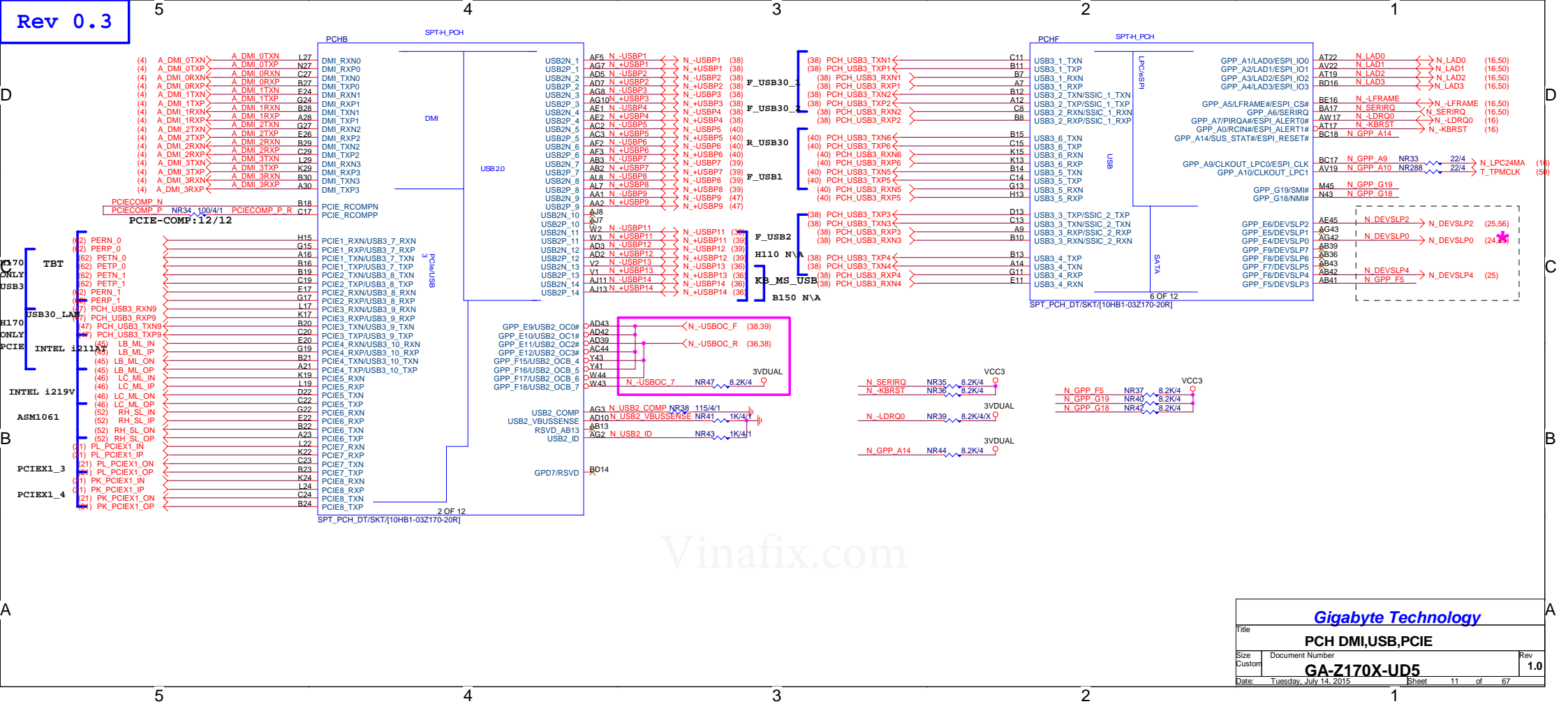
GA-Z170X-UD5

Rev: 1.0



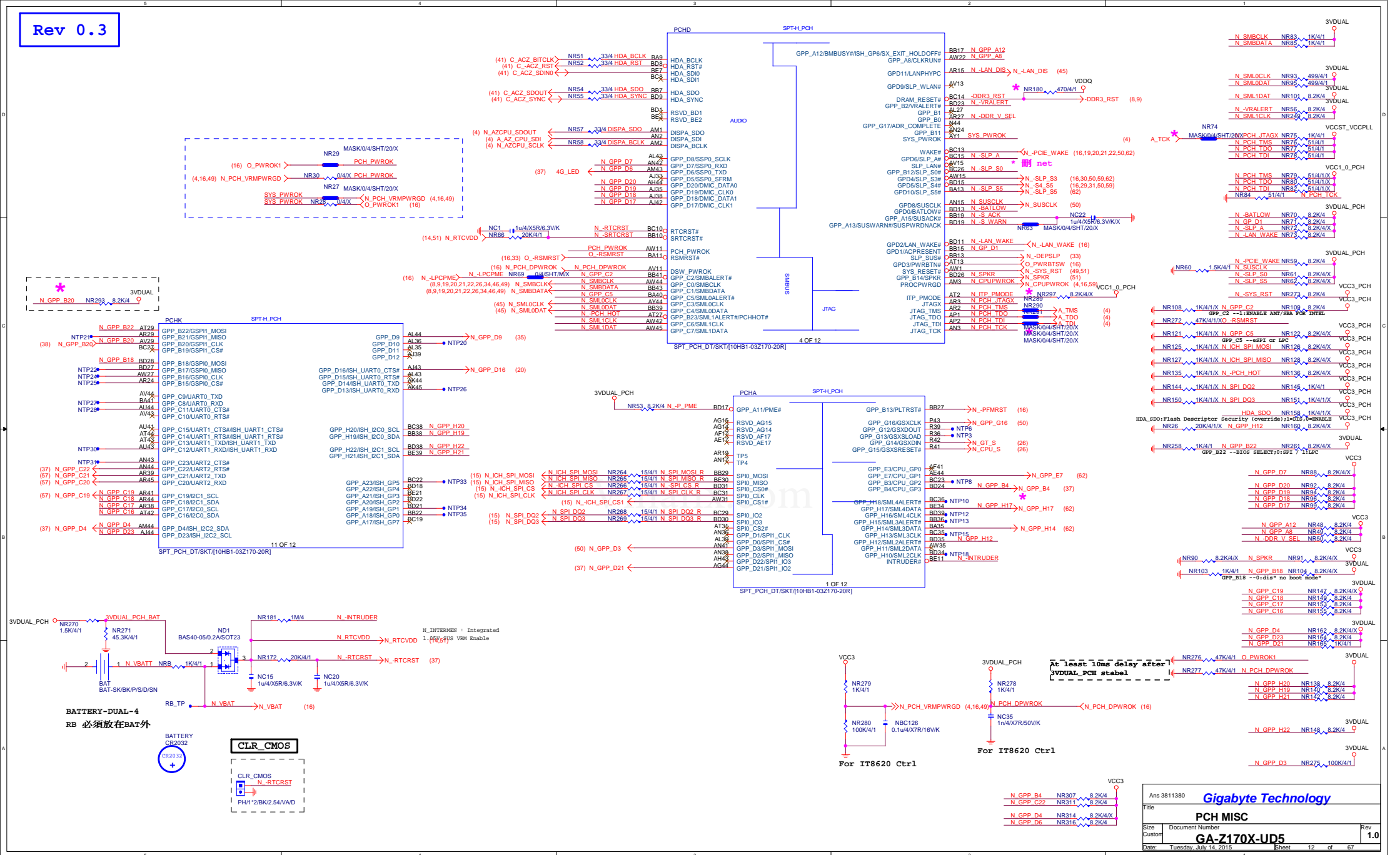
Rev 0.3



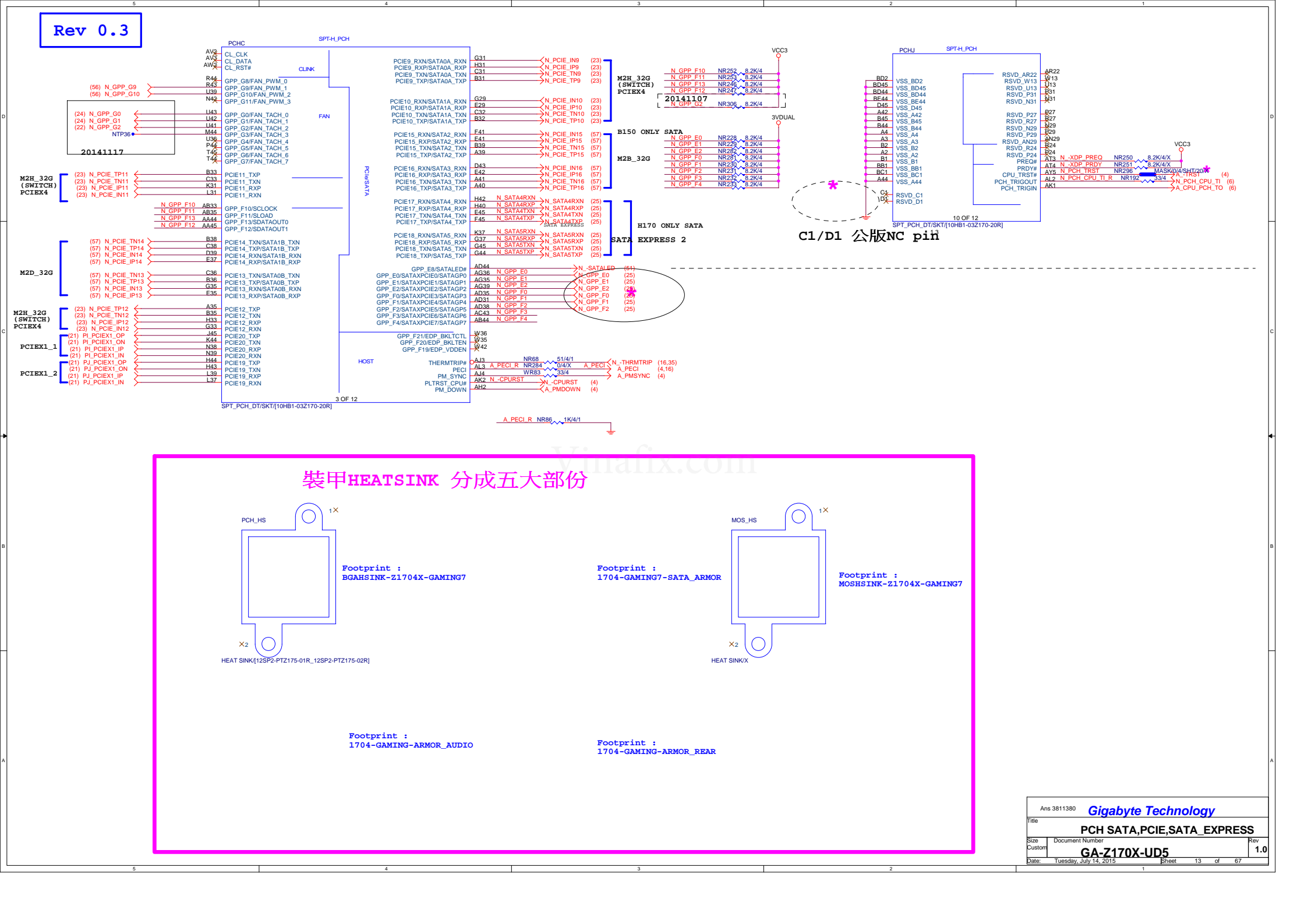


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Gigabyte Technology			
PCH DMI,USB,PCIE			
GA-Z170X-UD5	Rev 1.0		
Date: Tuesday, July 14, 2015	Sheet 11 of 67		



Rev 0.3



裝甲HEATSINK 分成五大部份

Footprint :
BGAHSINK-Z1704X-GAMING7

Footprint :
1704-GAMING7-SATA_ARMOR

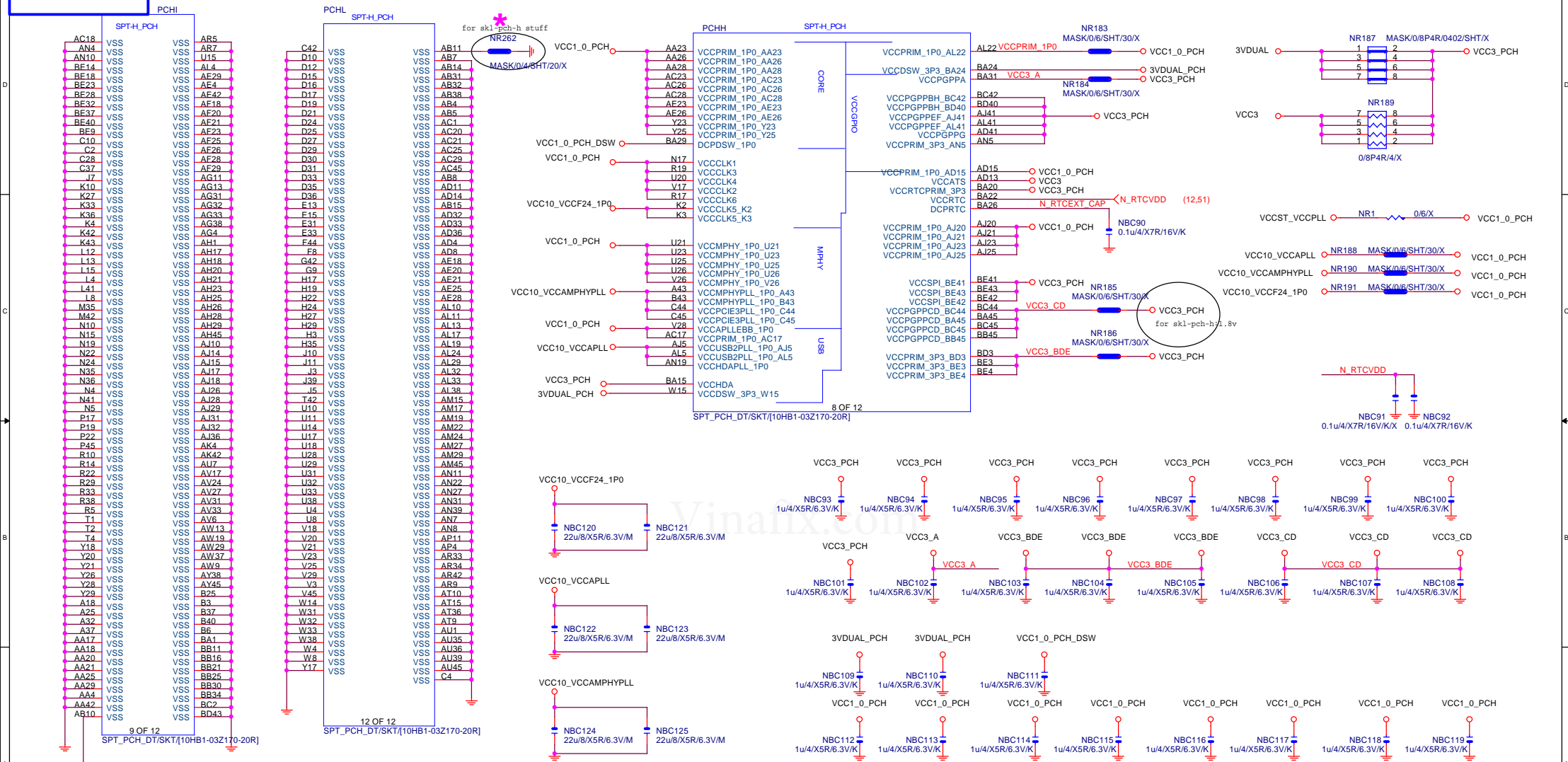
Footprint :
MOSH Sink-Z1704X-GAMING7

Footprint :
1704-GAMING-ARMOR_AUDIO

Footprint :
1704-GAMING-ARMOR_REAR

Footprint :
1704-GAMING-ARMOR_AUDIO

Footprint :
1704-GAMING-ARMOR REAR



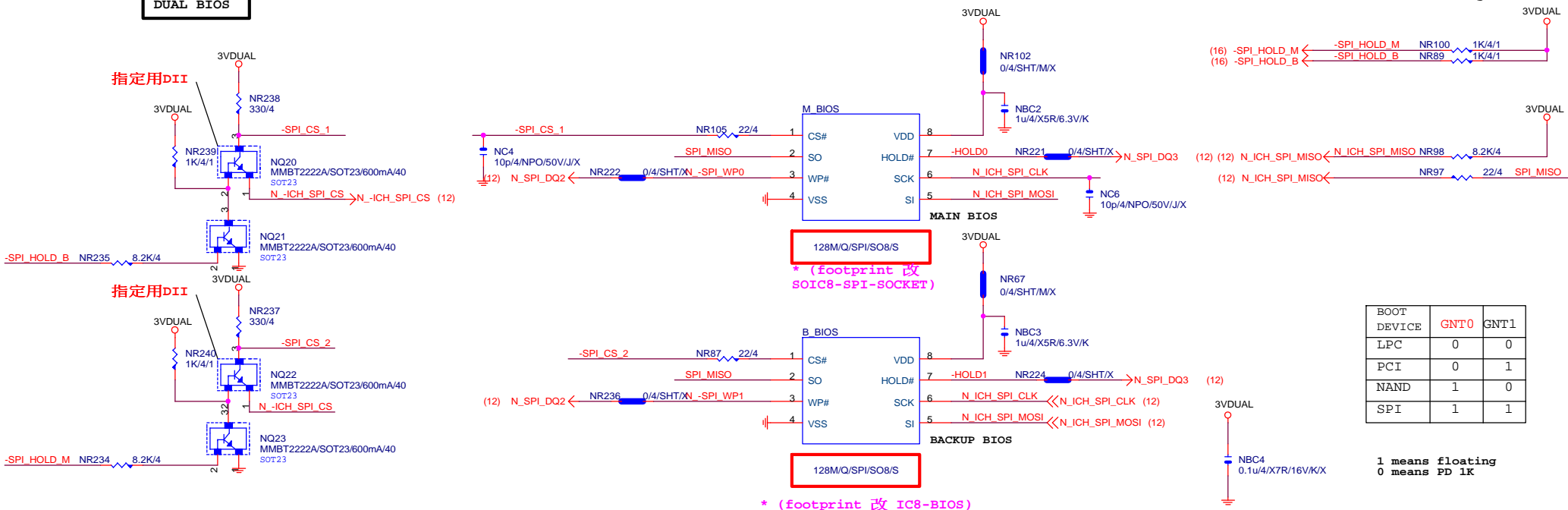
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DUAL BIOS

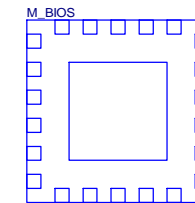
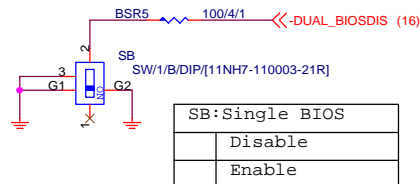
MOSI For DMI RX Termination Voltage

指定用DII

指定用DII



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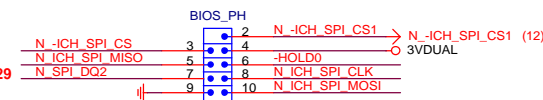


LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-31R]X

* 試産先上, PVT 移除

BIOS_PH

★Update 2015-01.29



MASK/PH/2*5K10/BK/2.54/VA/D/X

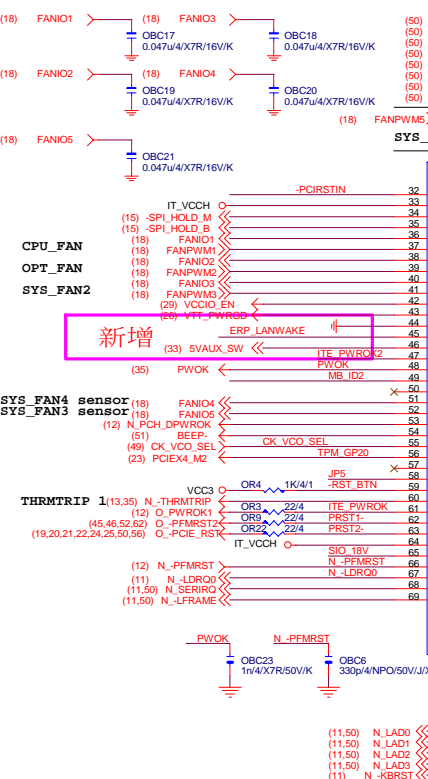
Footprint the same, confirmed by Graceing.

Use COM port pin header part.

Gigabyte Technology

Title	BIOS		
Size	Document Number	GA-Z170X-UD5	Rev 1.0
Date:	Tuesday, July 14, 2015	Sheet 15 of 67	

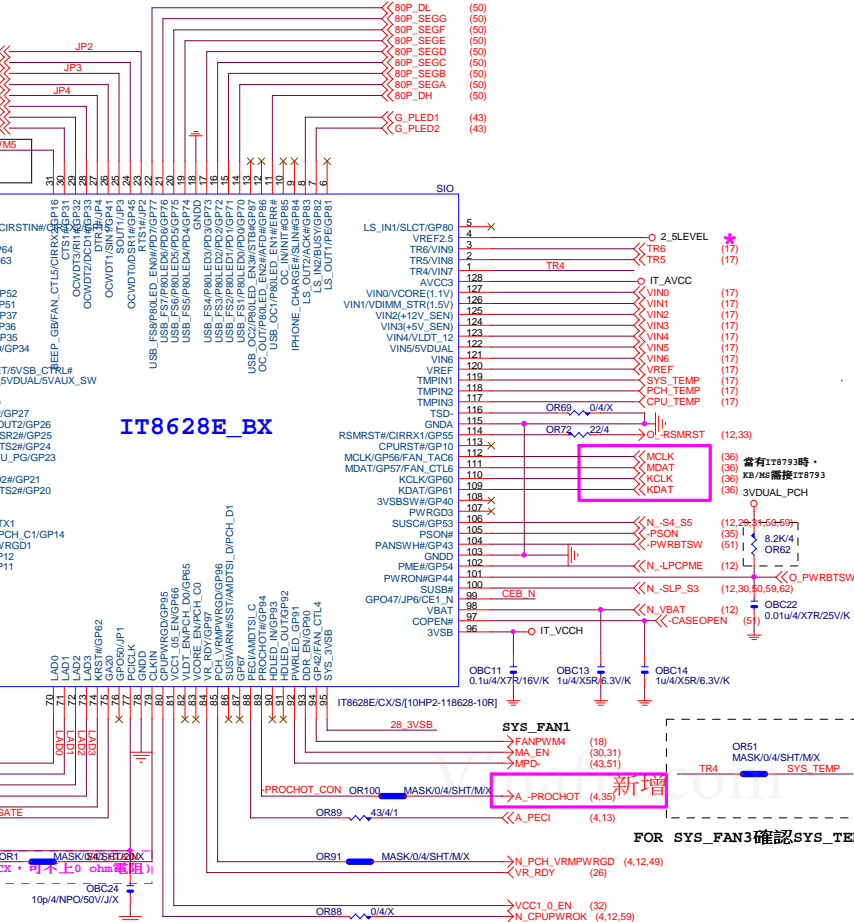
SIO IT8628BX REV:1.05



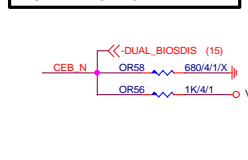
Placement CPU
(4) A_THRMTRIP WR10 1K/4/1 N_THRMTRIP
CPU 端 A_THRMTRIP不可與PCH及SIO N_THRMTRIP直接連接。否則會出現無法拉Low情況。

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL4 FAN_TAC4
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL5 FAN_TAC5
OPT_FAN	FAN_CTL2 FAN_TAC2
THRMTRIP1	YES PIN60

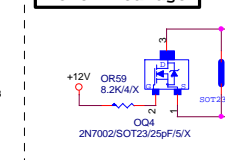
IT8620E GPIO問題匯整	
PIN 50	GP26-第一次接上POWER時會拉 Lo
PIN 90/91	DEFAULT為HDLed FUNCTION, GP93 BYPASS TO GP92 高電阻時 GP92 會被拉Lo(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 Lo
PIN 111/112	MOUSE 跟PAN6 FUNCTION 擇一使用, 不然會互相干擾
PIN 22	PIN22, 需高於3V, 若低於該部分COM PORT及LPT裝置蜂鳴器會異常動作。



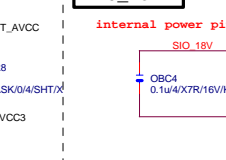
DUAL BIOS OPT STRAP



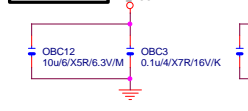
Power leakage



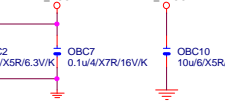
SIO_18V



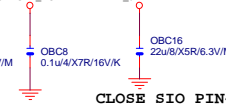
SIO CAP



IT_VCCB



IT_AVCC



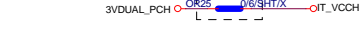
3VDUAL_PCH



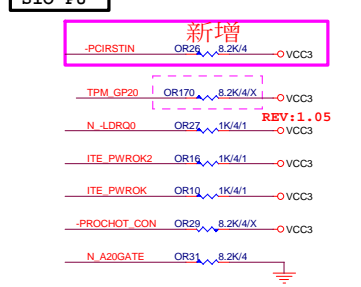
2.5LEVEL



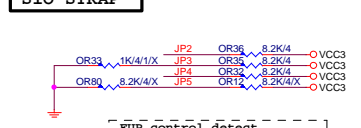
PWR SHT



SIO PU

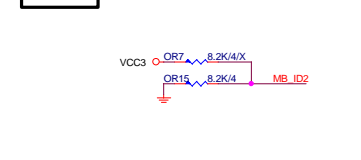


SIO STRAP



JP2	1	Disable WDT
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual BIOS CS PIN Disable
JP3	0	Dual BIOS CS PIN Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

MB ID

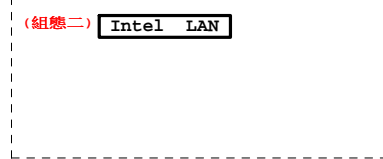


ERP WAKE on LAN (依LAN組態選擇)

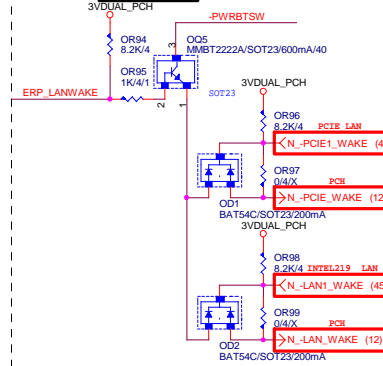
(組態一) Realtek/ATHEROS LAN



(組態二) Intel LAN

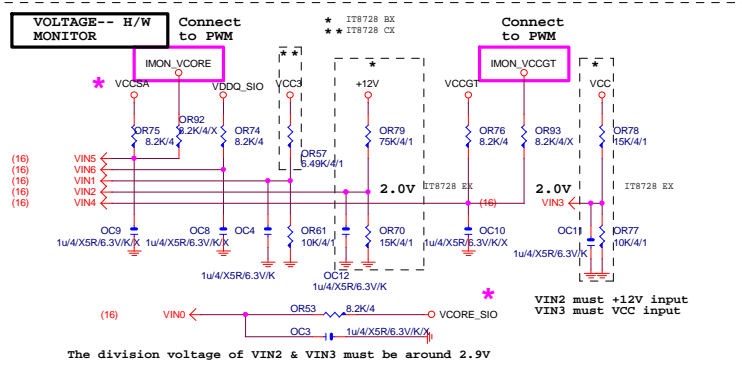
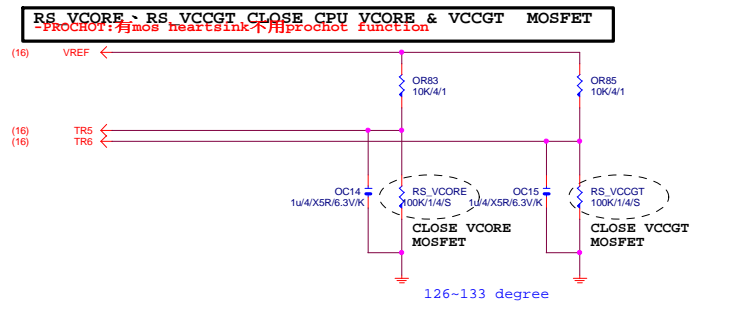
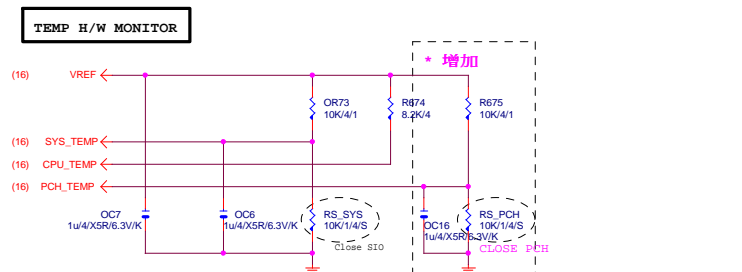


(組態三) Dual LAN

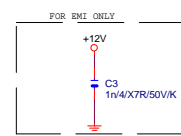


ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN	Atheros+Atheros	組態一
	Intel 219+Atheros	組態三
No Support ERP	Intel 219+Intel 210	組態三
	BOM不上	N/A

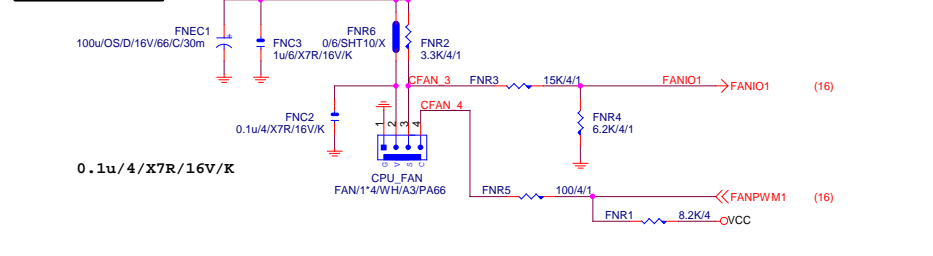
Gigabyte Technology		
ITE 8620 LPC IO		
Size Custom	Document Number	Rev 1.0
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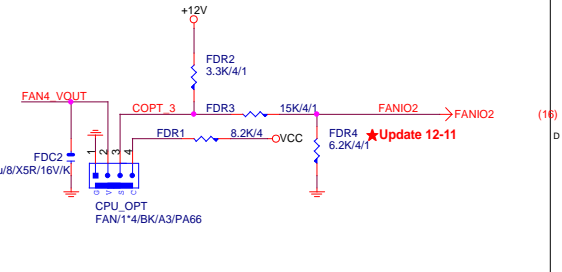
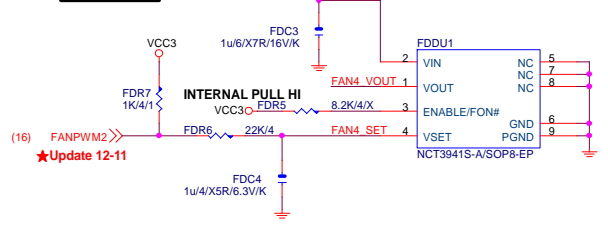
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CPU SMART FAN

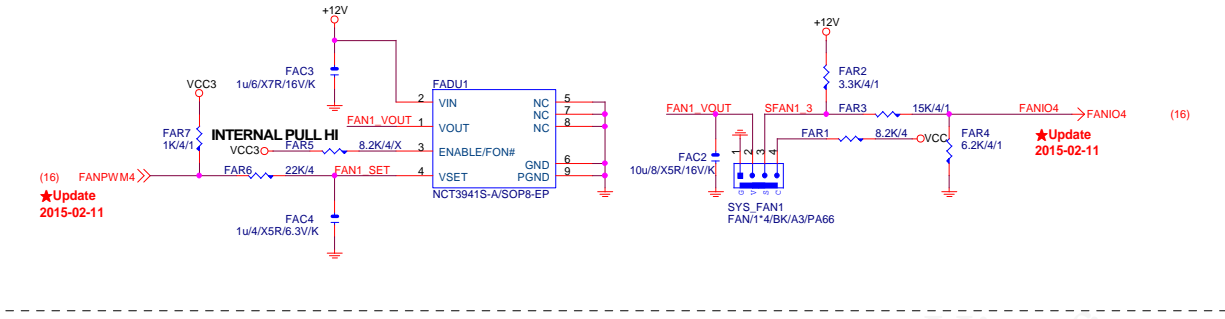


CPU_OPT



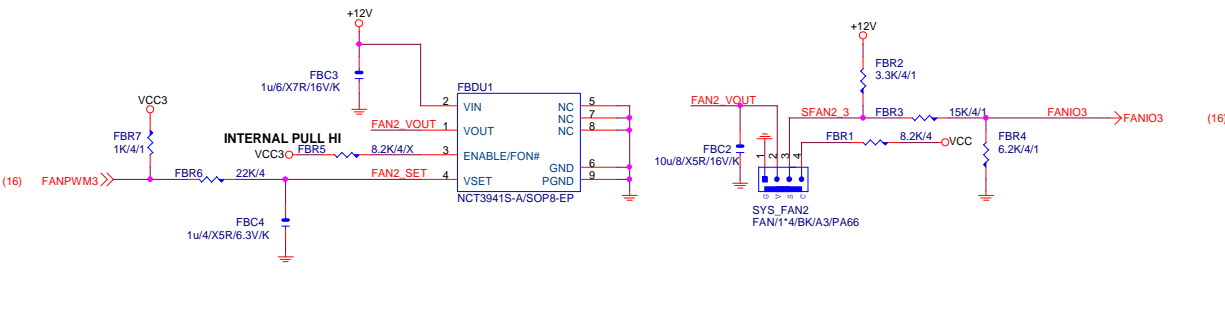
SYSTEM FAN1

Linear SYS_FAN
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)

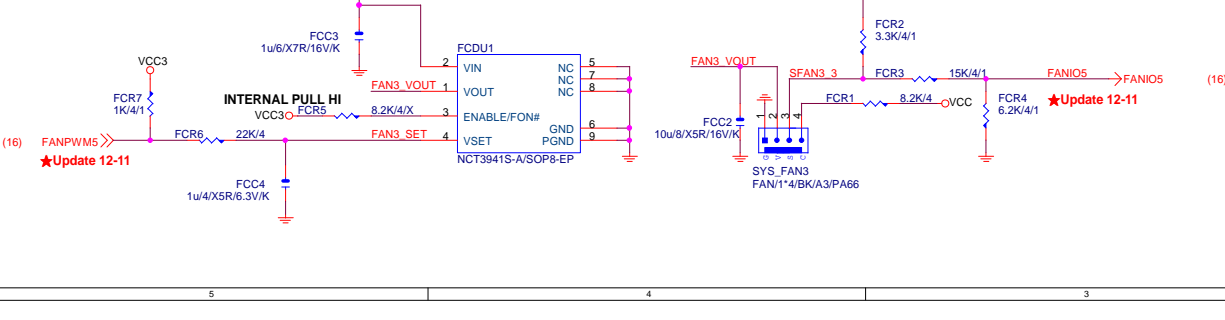


SYSTEM FANX

SYSTEM FAN2



SYSTEM FAN3

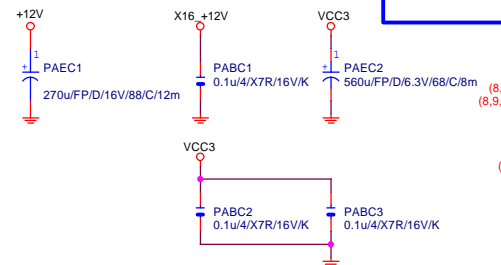


PCIEX16 CAP

Rev 0.3

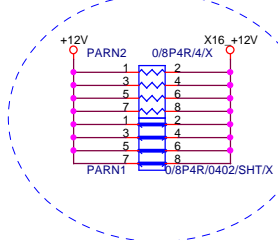
PCIEX16 SLOT

PCIESLOT-164STH



PCIEX16 PROTECT SHT

+12 protect short-wire test



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4X5R/6.3V/K	PA EXP SW TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHZ*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHZ*(8b/10b)X2=4Gb/s=500MB/s

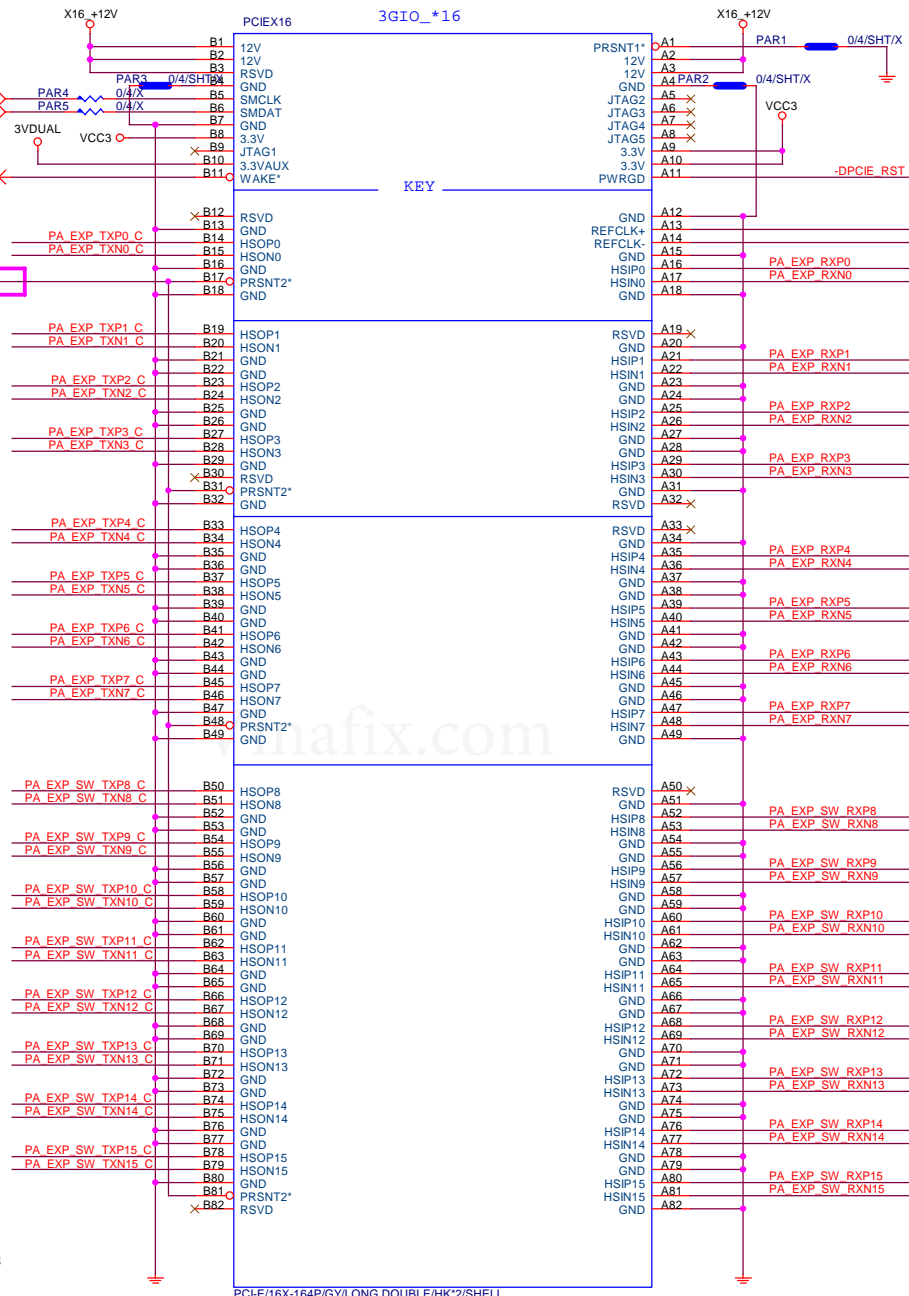
PCE-E X16(單向) BANDWITH=2.5GHZ*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHZ*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

(12,16,20,21,22,50,52) N_-PCIE_WAKE

(10) -PCIE16_PR



PCI-E/16X-164P/GY/LONG DOUBLE/HK*2/SHELL

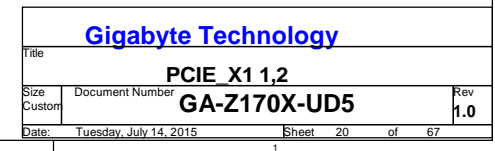
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PCIEX16:16/5/5/5/16

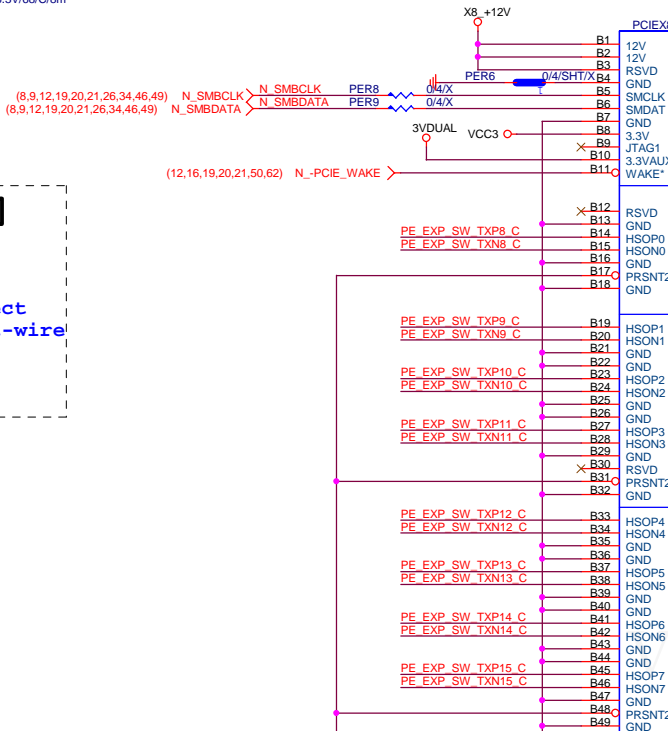
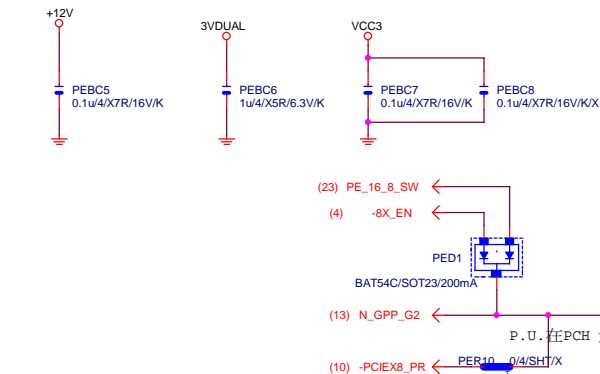
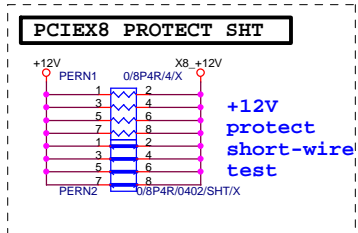
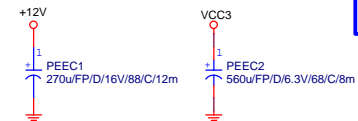
PA EXP RXP0.15]	>>>PA_EXP_RXP0[0.15]	(4,23)
PA EXP RXN0.15]	>>>PA_EXP_RXN0[0.15]	(4,23)
PA EXP TXP0.15]	>>>PA_EXP_TXP0[0.15]	(4,23)
PA EXP TXN0.15]	>>>PA_EXP_TXN0[0.15]	(4,23)
PA EXP SW RXP8.15]	>>>PA_EXP_SW_RXP8[8.15]	(23)
PA EXP SW RXN8.15]	>>>PA_EXP_SW_RXN8[8.15]	(23)
PA EXP SW TXP8.15]	>>>PA_EXP_SW_TXP8[8.15]	(23)
PA EXP SW TXN8.15]	>>>PA_EXP_SW_TXN8[8.15]	(23)

Gigabyte Technology

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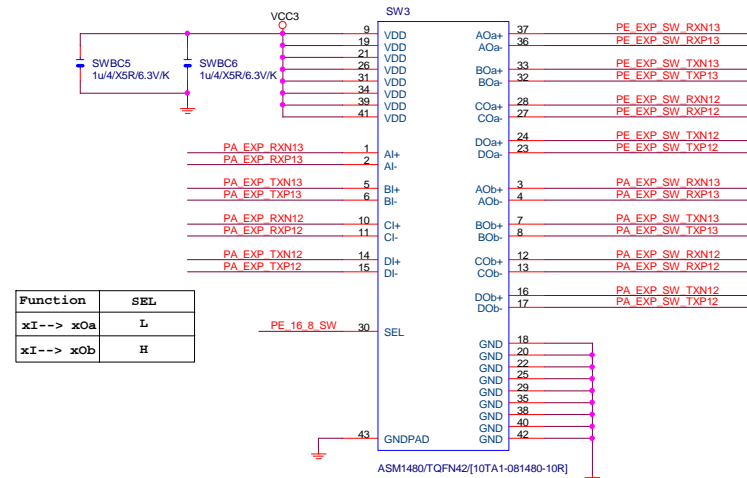
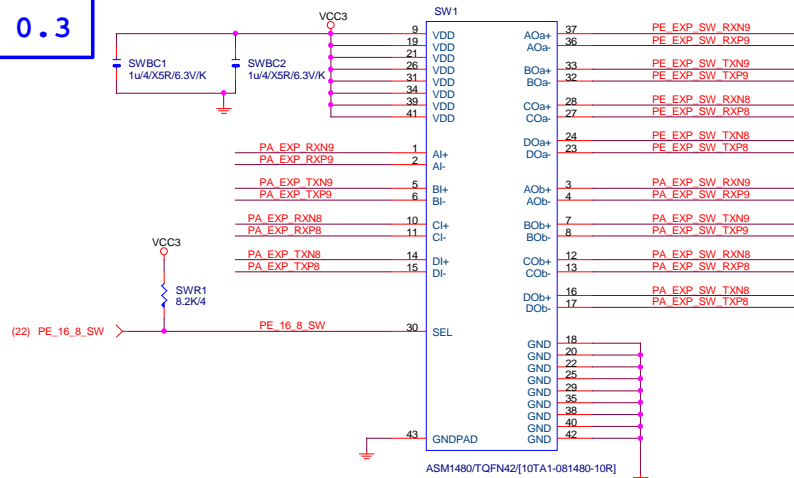
Rev 0.3



PCI-E/8X-99P/GY/LONG DOUBLE/HK*2/SHELL

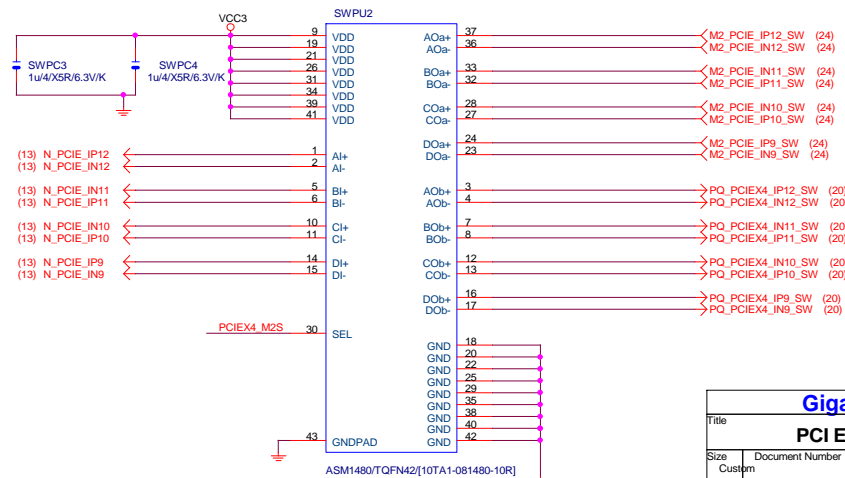
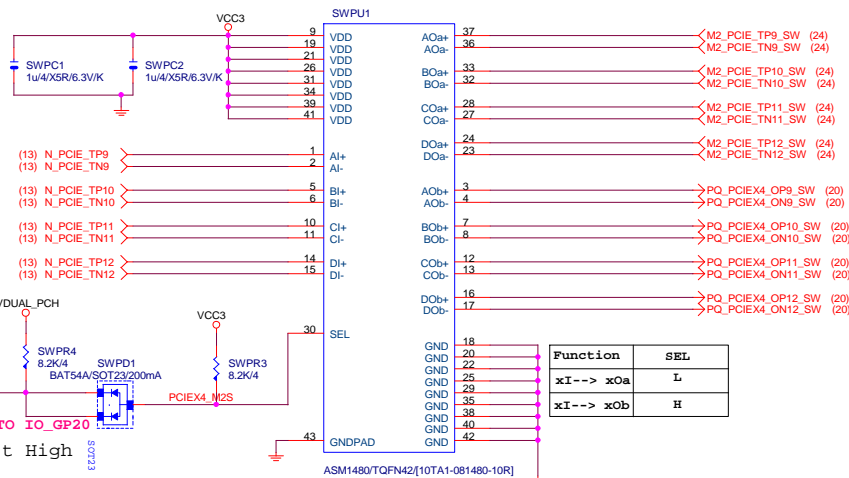
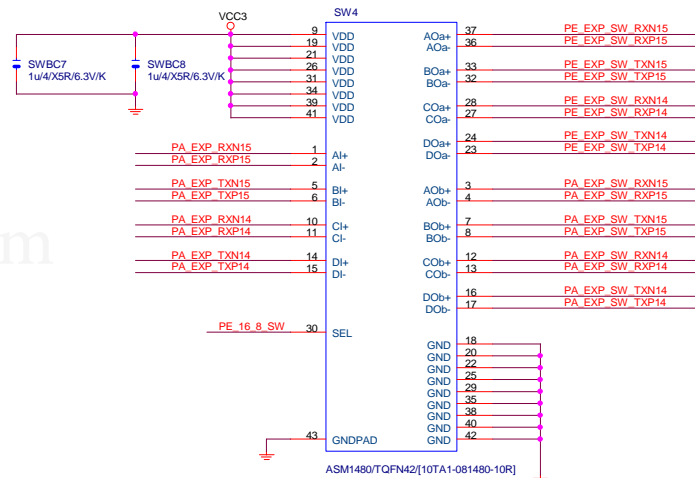
PE EXP SW TXP8	PEC7	0.22u4/X5R/6.3V/K	PE EXP SW TXP8_C
PE EXP SW TXN8	PEC8	0.22u4/X5R/6.3V/K	PE EXP SW TXN8_C
PE EXP SW TXP9	PEC9	0.22u4/X5R/6.3V/K	PE EXP SW TXP9_C
PE EXP SW TXN9	PEC10	0.22u4/X5R/6.3V/K	PE EXP SW TXN9_C
PE EXP SW TXP10	PEC11	0.22u4/X5R/6.3V/K	PE EXP SW TXP10_C
PE EXP SW TXN10	PEC12	0.22u4/X5R/6.3V/K	PE EXP SW TXN10_C
PE EXP SW TXP11	PEC13	0.22u4/X5R/6.3V/K	PE EXP SW TXP11_C
PE EXP SW TXN11	PEC14	0.22u4/X5R/6.3V/K	PE EXP SW TXN11_C
PE EXP SW TXP12	PEC15	0.22u4/X5R/6.3V/K	PE EXP SW TXP12_C
PE EXP SW TXN12	PEC16	0.22u4/X5R/6.3V/K	PE EXP SW TXN12_C
PE EXP SW TXP13	PEC17	0.22u4/X5R/6.3V/K	PE EXP SW TXP13_C
PE EXP SW TXN13	PEC18	0.22u4/X5R/6.3V/K	PE EXP SW TXN13_C
PE EXP SW TXP14	PEC19	0.22u4/X5R/6.3V/K	PE EXP SW TXP14_C
PE EXP SW TXN14	PEC20	0.22u4/X5R/6.3V/K	PE EXP SW TXN14_C
PE EXP SW TXP15	PEC21	0.22u4/X5R/6.3V/K	PE EXP SW TXP15_C
PE EXP SW TXN15	PEC22	0.22u4/X5R/6.3V/K	PE EXP SW TXN15_C

Gigabyte Technology			
Title			
PCI EXPRESS X8			
Size	Document Number	GA-Z170X-UD5	Rev
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Function	SEL
xI--> xOa	L
xI--> xOb	H

PA EXP SW RXP18_15I >>> PA_EXP_SW_RXP18_15I (19)
PA EXP SW RXN18_15I >>> PA_EXP_SW_RXN18_15I (19)
PA EXP SW TXP18_15I >>> PA_EXP_SW_TXP18_15I (19)
PA EXP SW TXN18_15I >>> PA_EXP_SW_TXN18_15I (19)
PE EXP SW RXP18_15I >>> PE_EXP_SW_RXP18_15I (22)
PE EXP SW RXN18_15I >>> PE_EXP_SW_RXN18_15I (22)
PE EXP SW TXP18_15I >>> PE_EXP_SW_TXP18_15I (22)
PE EXP SW TXN18_15I >>> PE_EXP_SW_TXN18_15I (22)
PA EXP RXP10_15I >>> PA_EXP_RXP10_15I (4,19)
PA EXP RXN10_15I >>> PA_EXP_RXN10_15I (4,19)
PA EXP TXP10_15I >>> PA_EXP_TXP10_15I (4,19)
PA EXP TXN10_15I >>> PA_EXP_TXN10_15I (4,19)



M.2 Lane4 from PCH port18

(23) M2_PCIE_IN12_SW < M2HC33 M2_PCIE_TN12_SW_C
(23) M2_PCIE_IP12_SW < M2HC33 M2_PCIE_TP12_SW_C

M.2 Lane3 from PCH port17

(23) M2_PCIE_IN11_SW < M2HC35 M2_PCIE_TN11_SW_C
(23) M2_PCIE_IP11_SW < M2HC35 M2_PCIE_TP11_SW_C

M.2 Lane2 from PCH port16

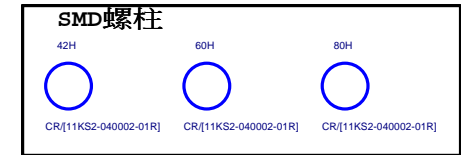
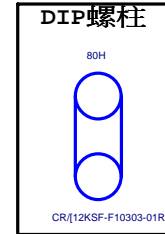
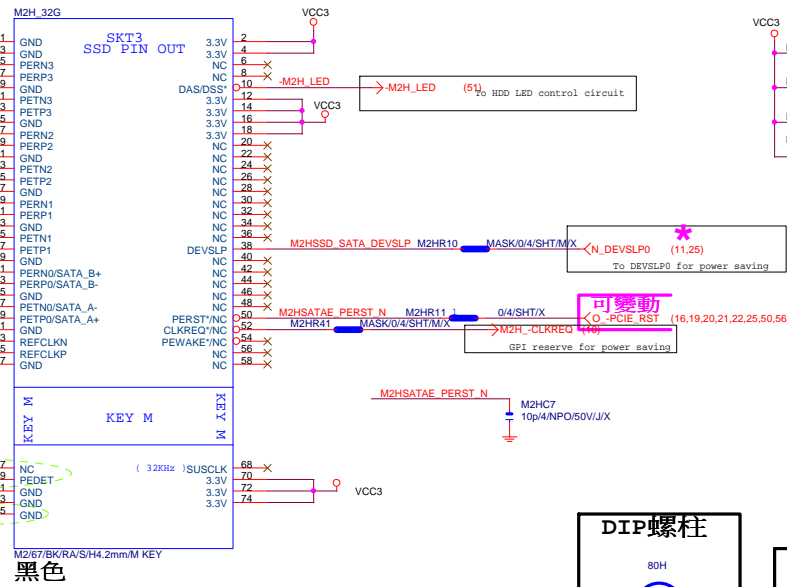
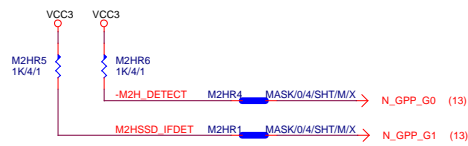
(23) M2_PCIE_IN10_SW < M2HC9 M2_PCIE_TN10_SW_C
(23) M2_PCIE_IP10_SW < M2HC9 M2_PCIE_TP10_SW_C

M.2 Lane2 from PCH port15

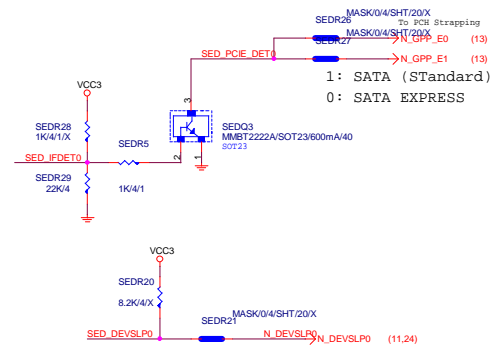
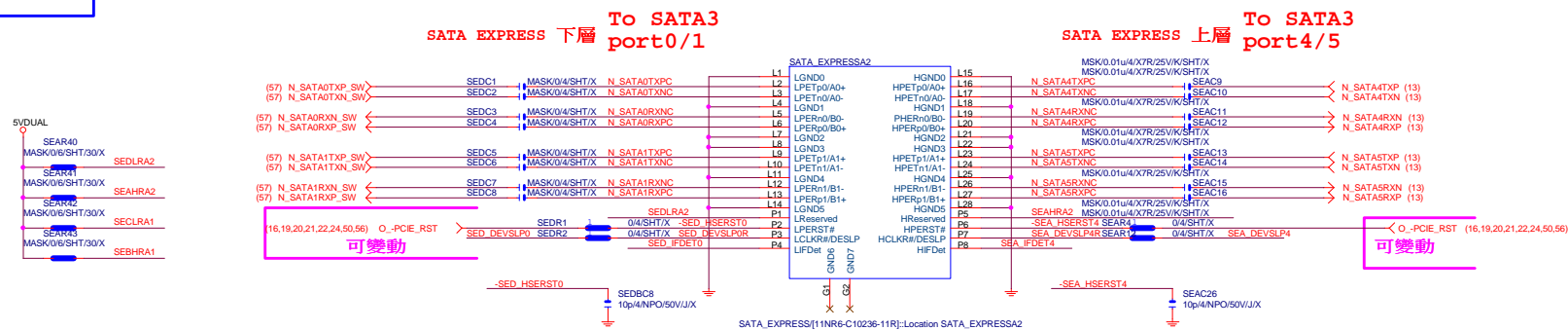
(23) M2_PCIE_IN9_SW < M2HC15 M2_PCIE_TN9_SW_C
(23) M2_PCIE_IP9_SW < M2HC15 M2_PCIE_TP9_SW_C

需與M2_-CLKREQ對應

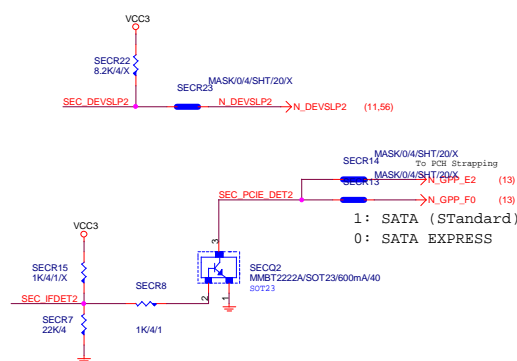
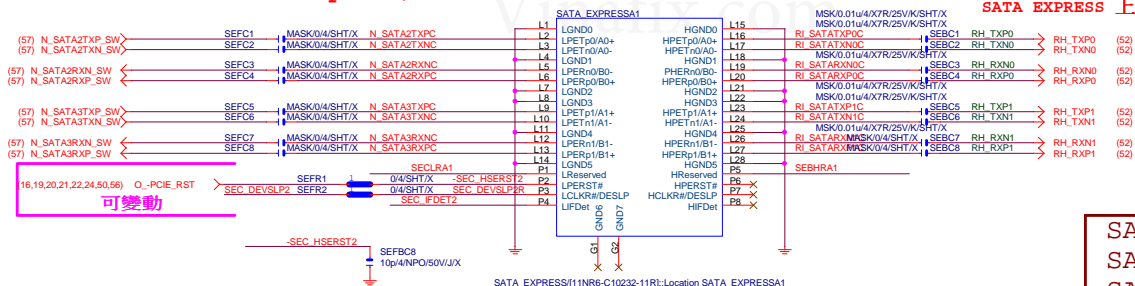
支援SATA and M.2 function



M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE X1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)		PCIE x4 (For M.2)			SATA	SATA
		SATA Express (Low)		PCIE x4 (For M.2)			SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)		PCIE x4			SATA	SATA
		SATA Express (Low)		PCIE x4			SATA Express	

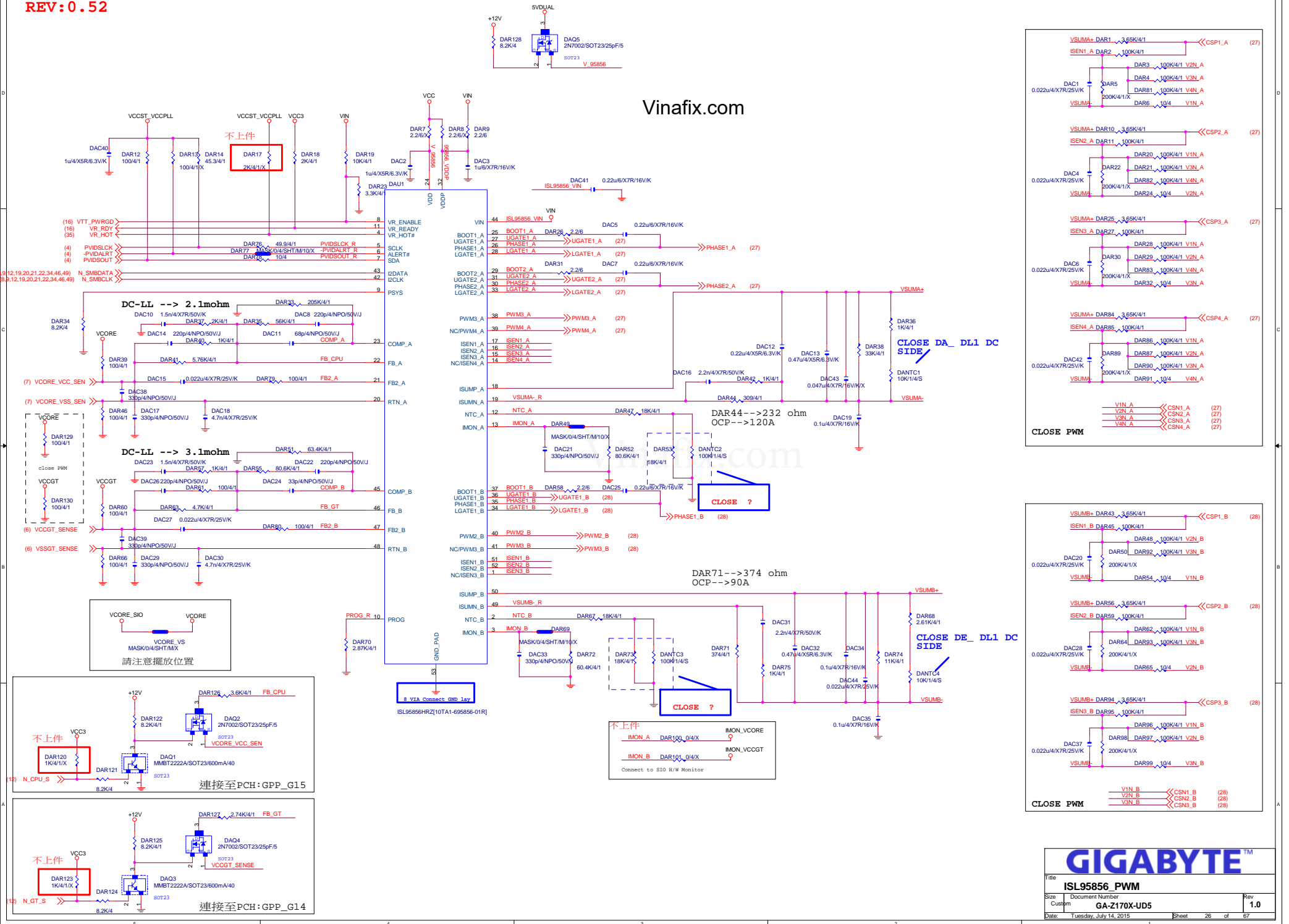


SATA EXPRESS 下層 To SATA3 port2/3

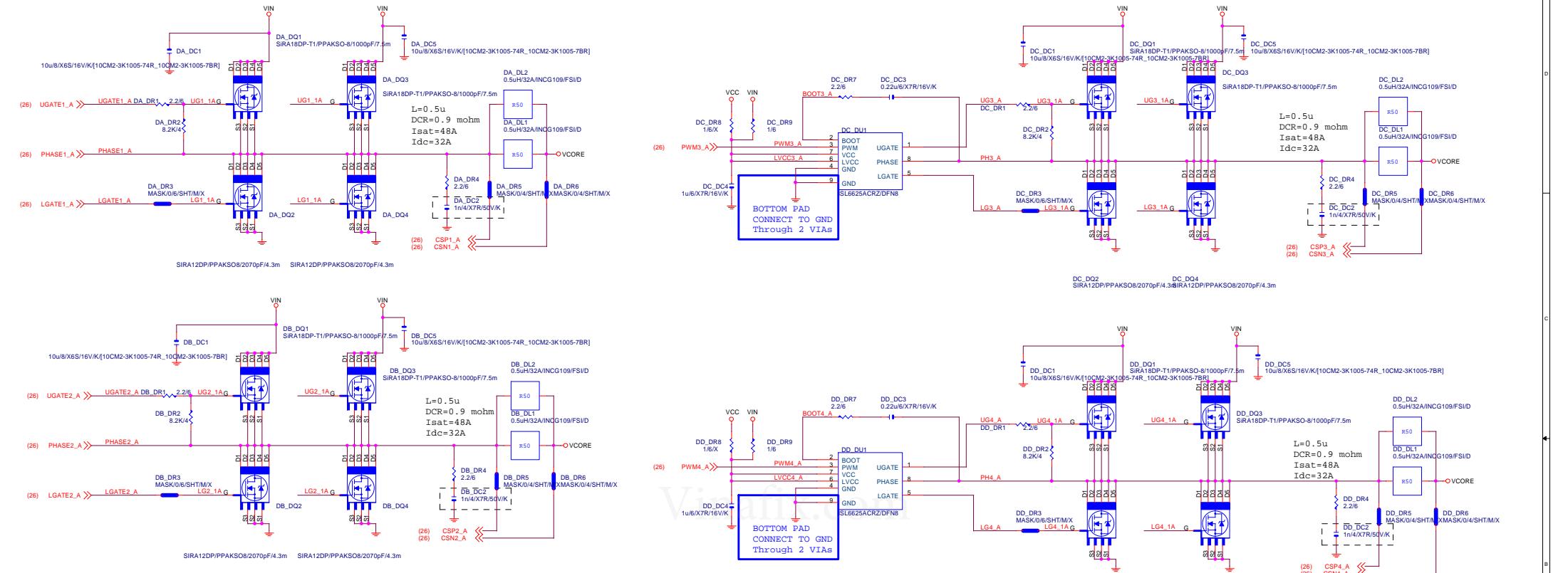


SATA 5 (文字面寫SATA 1)
 SATA 4 (文字面寫SATA 0)
 SATA 3
 SATA 2
 SATA 1 (文字面寫SATA 5)
 SATA 0 (文字面寫SATA 4)

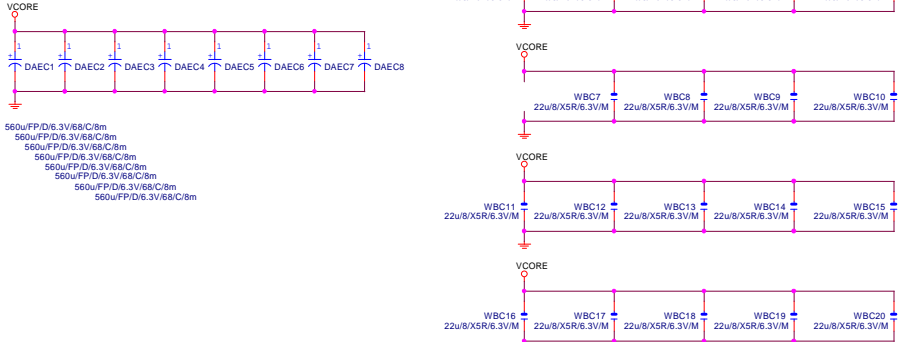
Vinafix.com



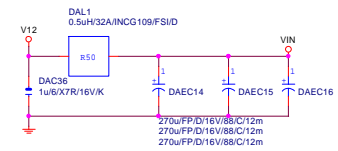
VCORE



VCORE CAP 560u*8PCS
22u*29PCS



VIN CAP 270u*3PCS



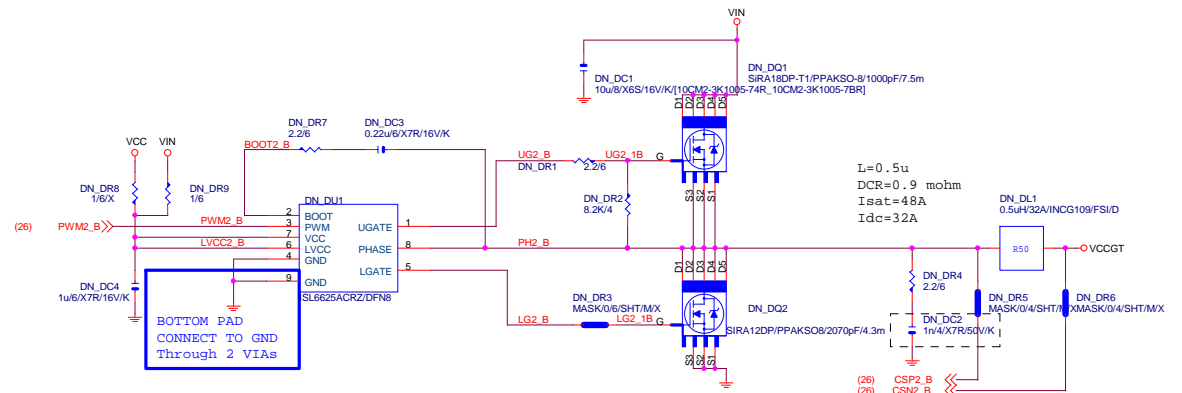
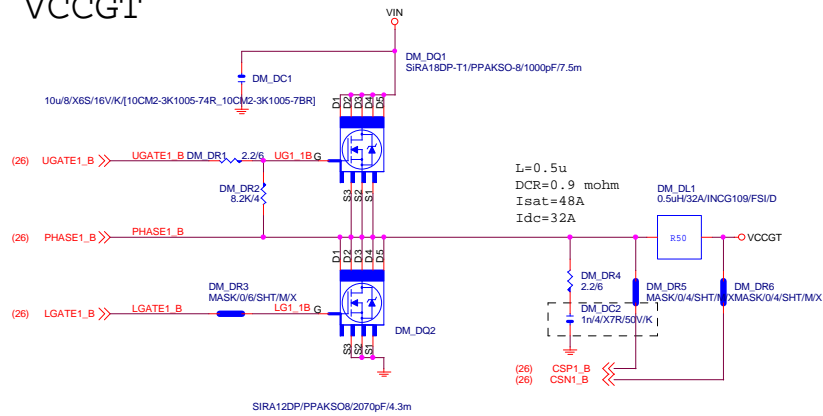
GIGABYTE™

ISL9585E MOS

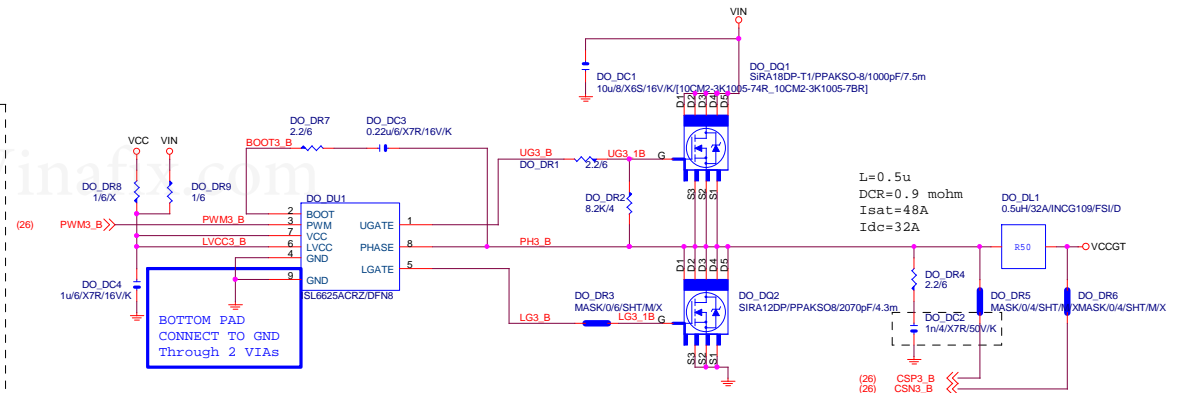
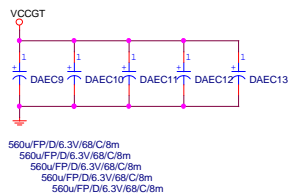
Size: Custom Document Number: GA-Z170X-UD5 Rev: 1.0

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VCCGT

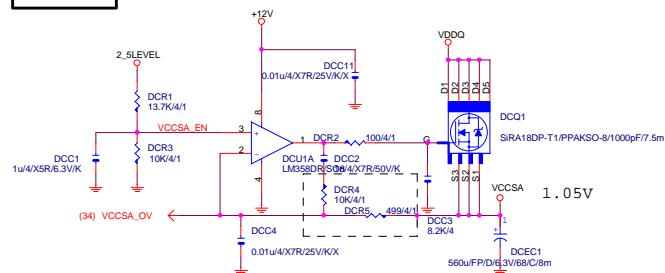


VCCGT CAP 560u*5PCS 22u*15PCS

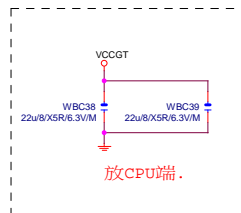
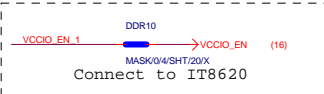
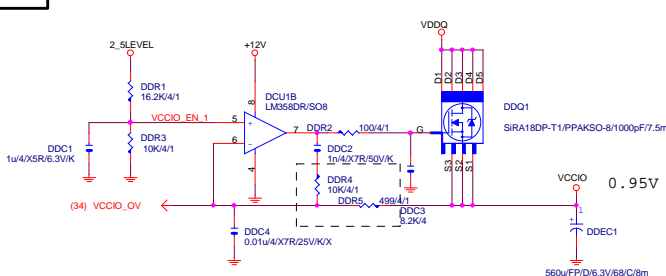


GIGABYTE™			
Title			
ISL95856 MOS			
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
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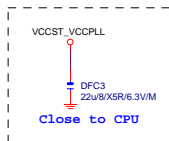
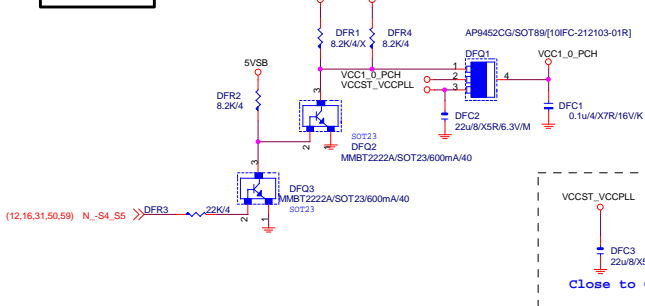
VCCSA



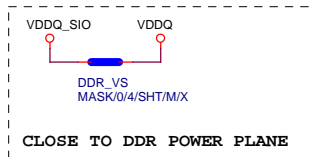
VCCIO



VCCST_VCCPLL

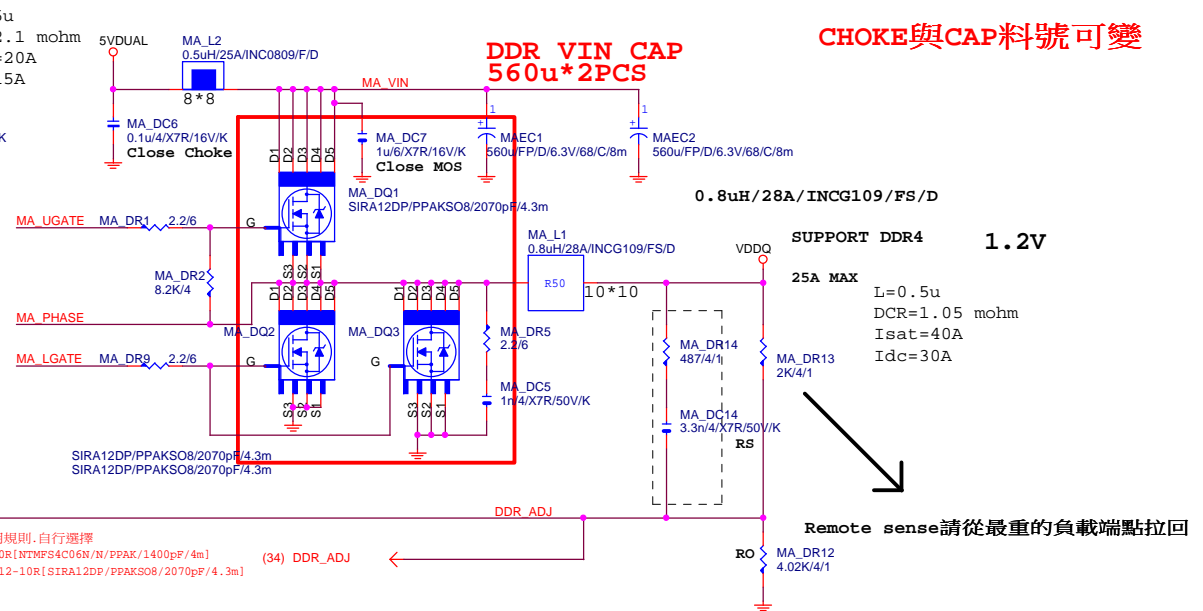


DDR4



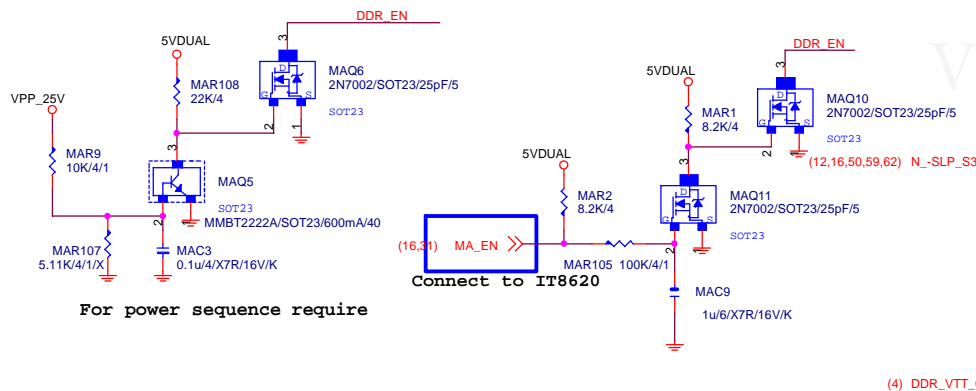
放靠近IC pin4

MOSFET請依MOSFET使用規則,自行選擇
ON-->10IF9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]
VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKS08/2070pF/4.3m]

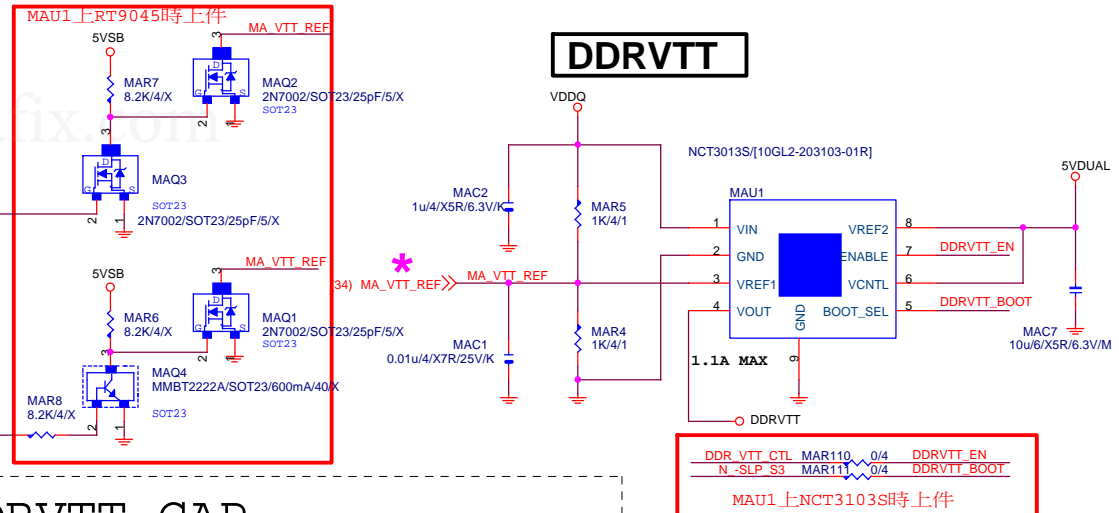


Remote sense請從最重的負載端點拉回

PWR SEQ



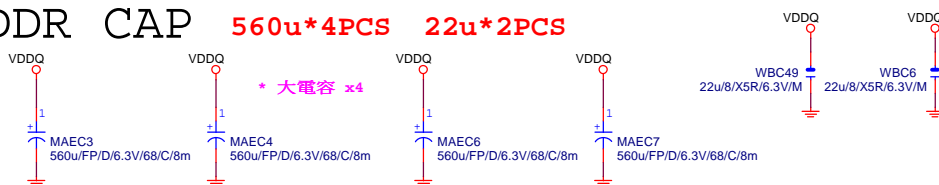
For power sequence require



DR VTT CTL MAR110 0/4 DDRVTT_EN
N -SLP S3 MAR111 0/4 DDRVTT_BOOT

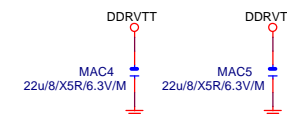
MAU1上NCT3103S時上件

DDRVTT CAP



* 大電容 x4

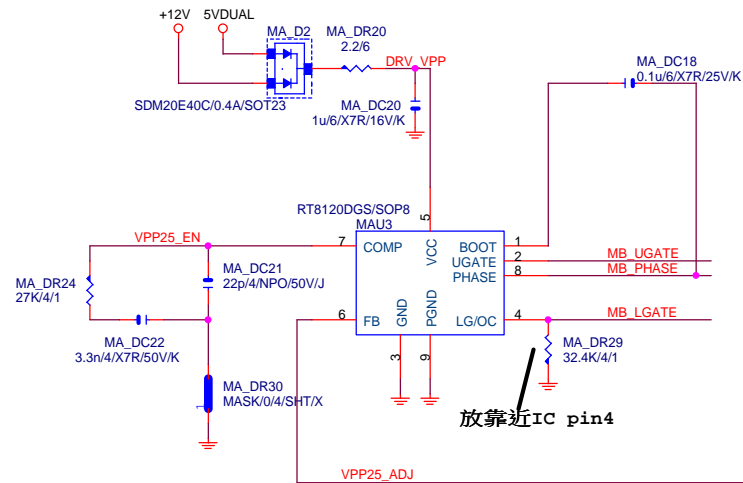
* 大電容 x0

**GIGABYTE™**

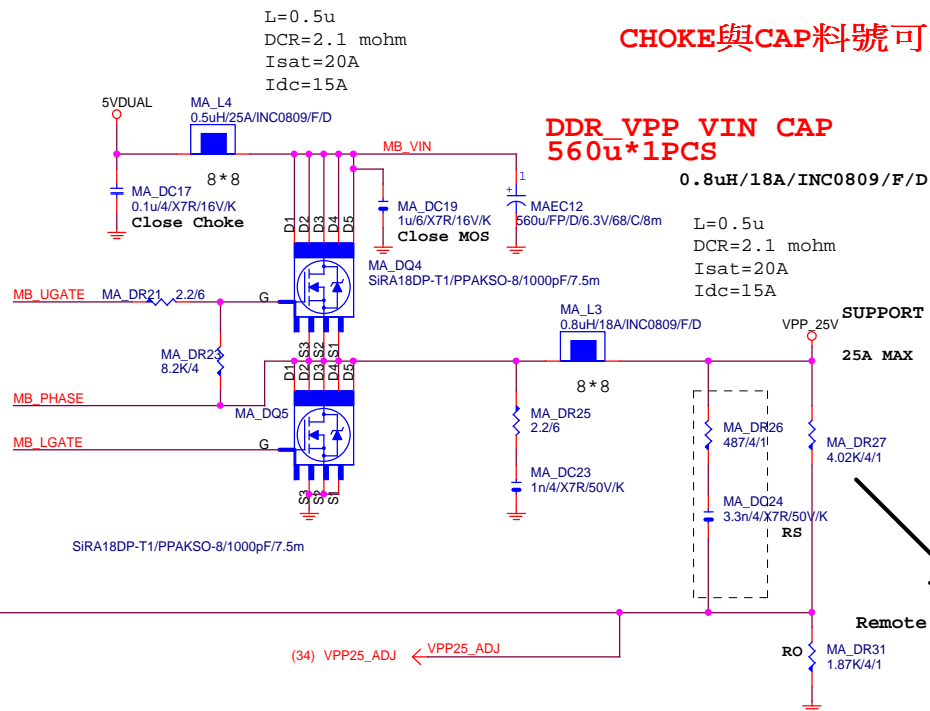
Title			
RT8120 DDR4 POWER			
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
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REV:0.83

VPP_25V



放靠近IC pin4

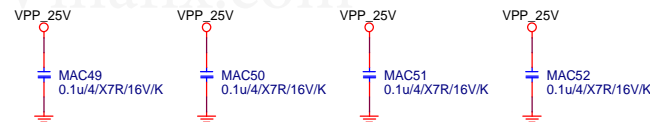
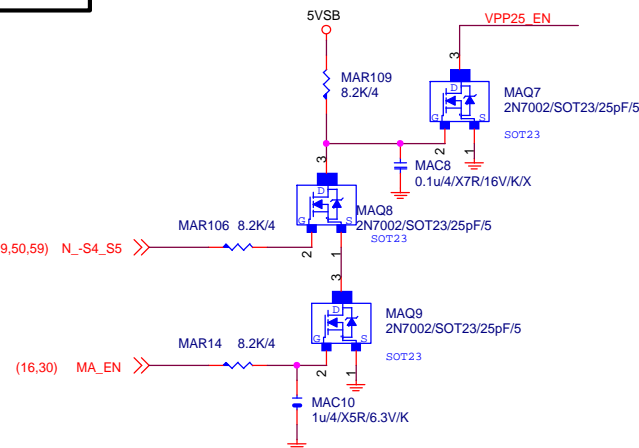


SUPPORT DDR4 2.5V

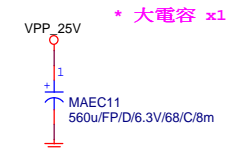
25A MAX

Remote sense請從最重的負載端點拉回

PWR_SEQ * 刪 MA_DR32



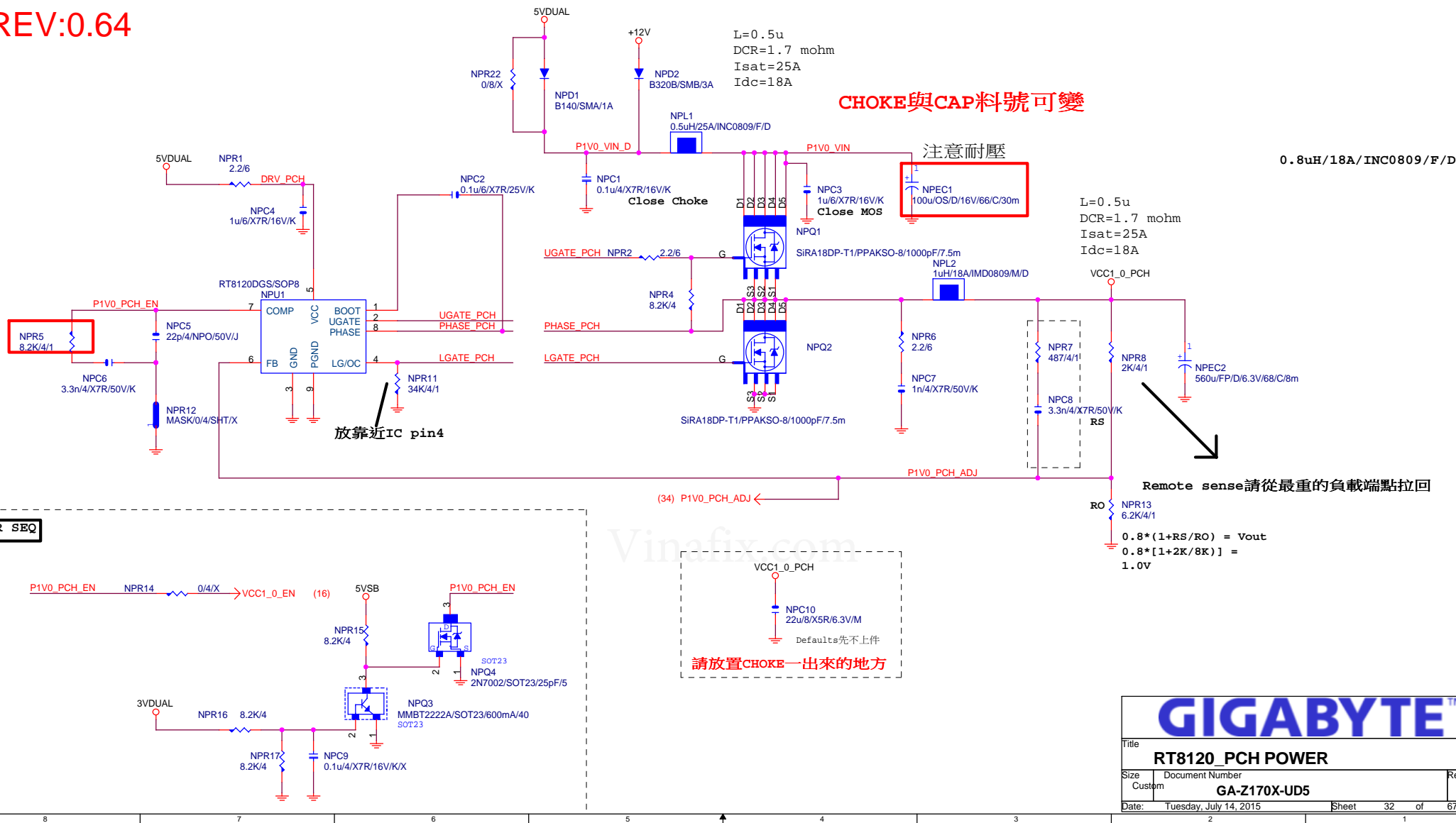
VPP CAP 560u*1PCS



* 大電容 x1

GIGABYTE™			
Title			
RT8120_VPP25 POWER			
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
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REV:0.64

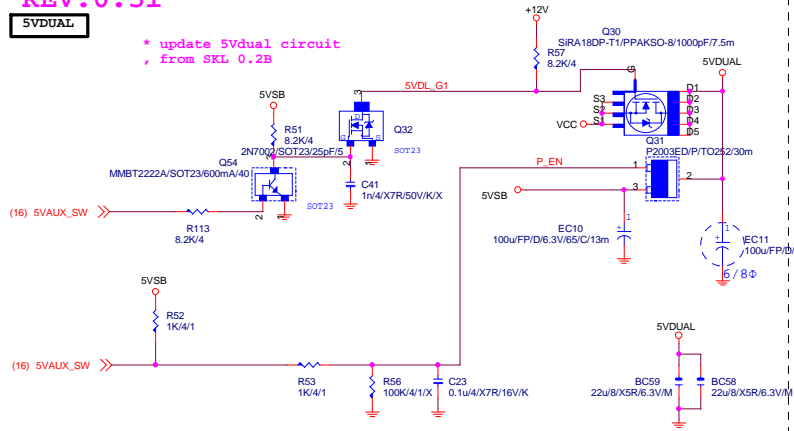


GIGABYTE™			
Title			
RT8120_PCH POWER			
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
Date:	Tuesday, July 14, 2015	Sheet	32 of 67

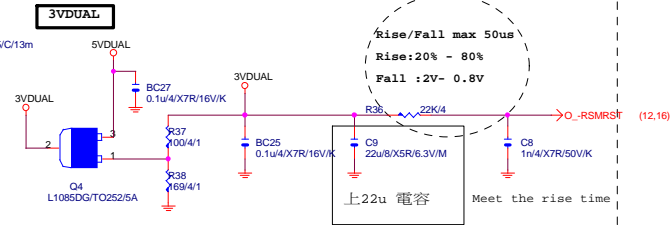
REV:0.51

5VDUAL

* update 5Vdual circuit
from SKL 0.2B



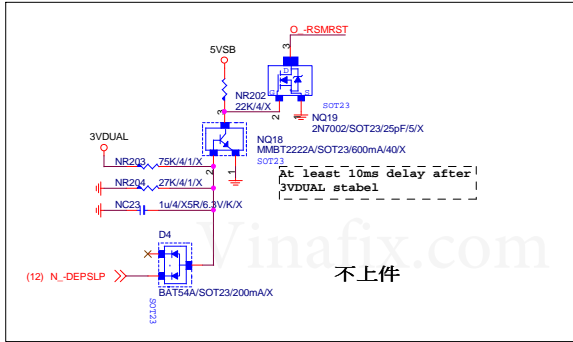
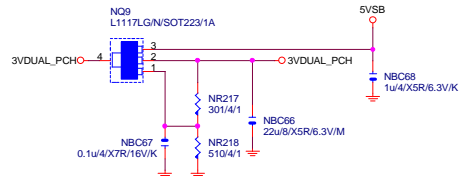
3VDUAL



Rise/Fall max 50us
Rise:20% - 80%
Fall :2V- 0.8V

上22u 电容
Meet the rise time

3VDUAL_PCH



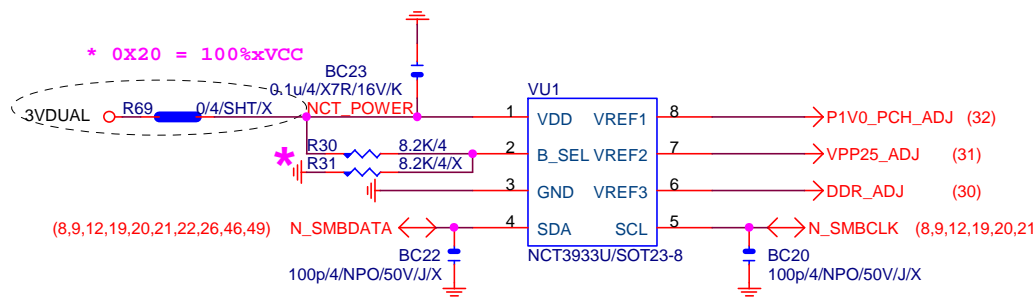
At least 10ms delay after
3VDUAL stabel

不上件

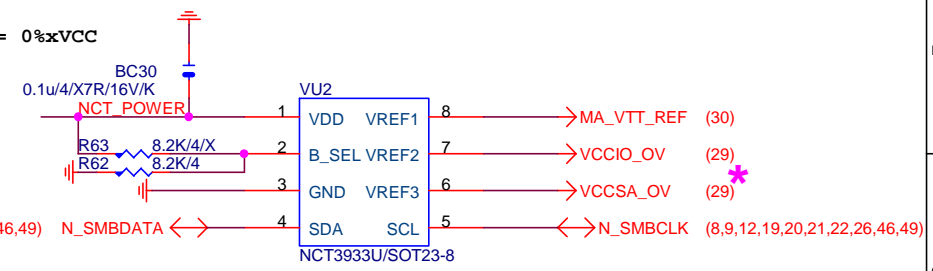
Gigabyte Technology

Title		
DISCRETE POWER		
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Custom	GA-Z170X-UD5	1.0
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OVER VOLTAGE



0X2A = 0%xVCC



0X22 = 75%xVCC

* 删除 OVU3

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

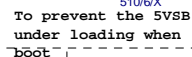
Gigabyte Technology

Title: CPU CORE VR-2

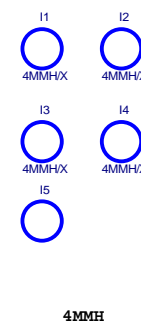
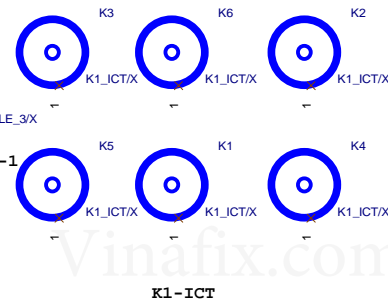
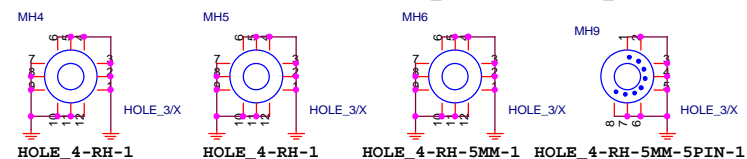
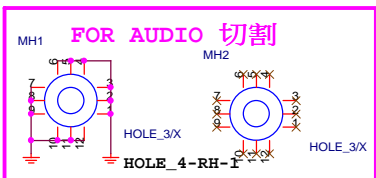
Size Custom	Document Number: GA-Z170X-UD5	Rev 1.0
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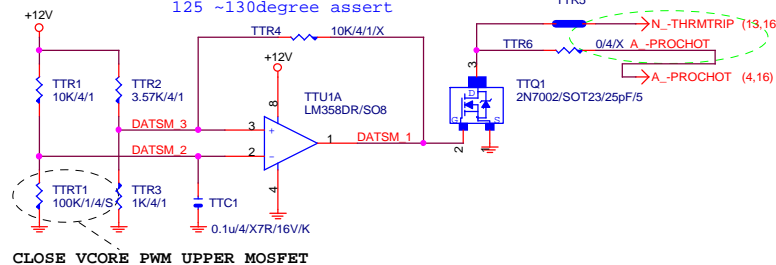
Patch some PSU no internal
pull up resistor



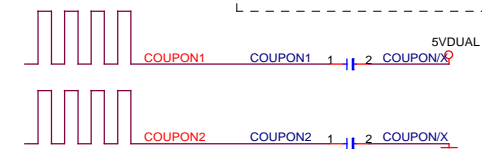
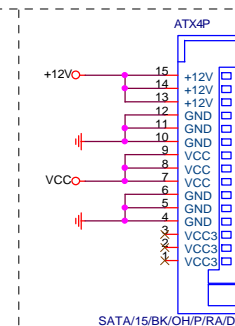
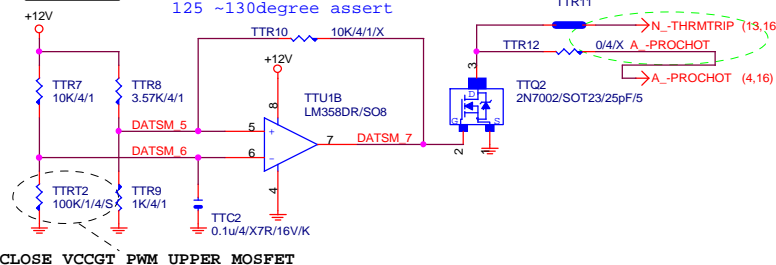
To fix 12V light load
abnromal issue



```
OTP:132度 / PCB THERMAL TRIP:122 度
125 ~130degree assert
```

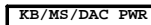
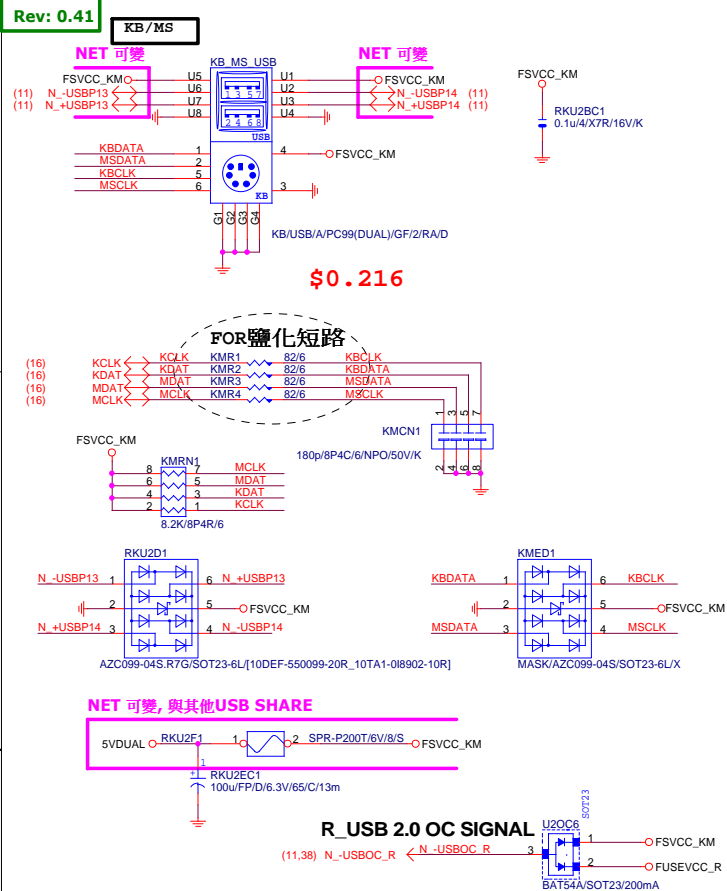


OTP:132度 / PCB THERMAL TRIP:122 度
125 ~130degree assert



Gigabyte Technology

Title			
ATX POWER CONNECTOR			
Size Custom	Document Number	GA-Z170X-UD5	Rev 1.0
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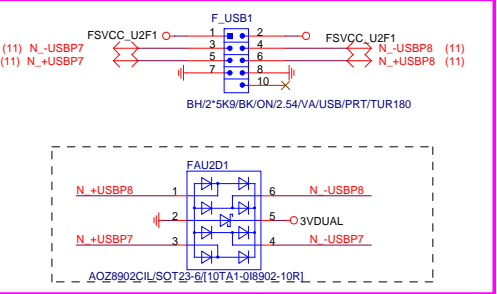




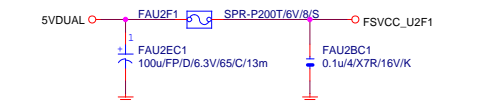
Vinafix.com

Gigabyte Technology			
OC BOTTOM			
Size Custom	Document Number	GA-Z170X-UD5	Rev 1.0
Date:	Tuesday, July 14, 2015	Sheet 37 of 67	

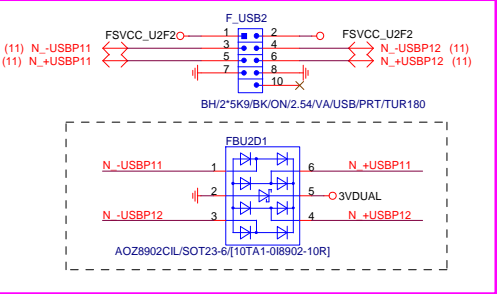
NET 可變



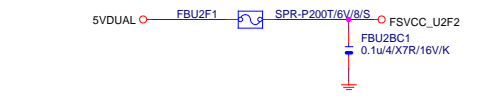
Close to connector
FUSE 2 Port 1 Fuse 2A



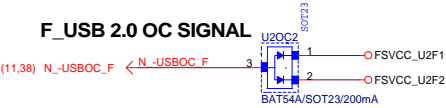
NET 可變



Close to connector
FUSE 2 Port 1 Fuse 2A

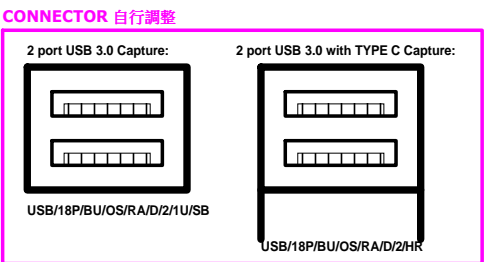
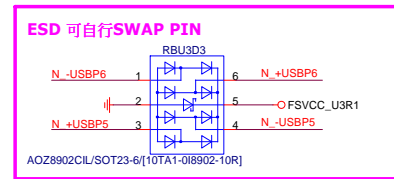
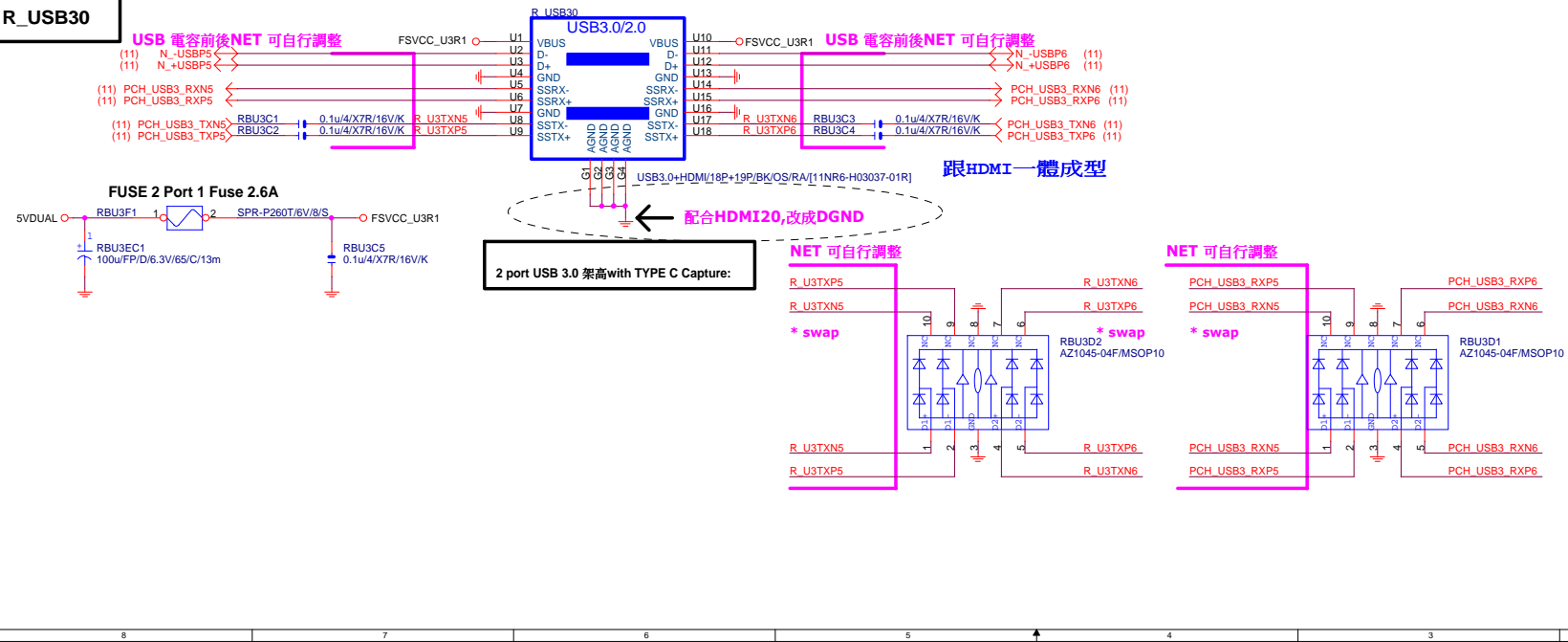


F_USB 2.0 OC SIGNAL



Vinafix.com

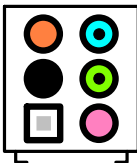
R_USB30



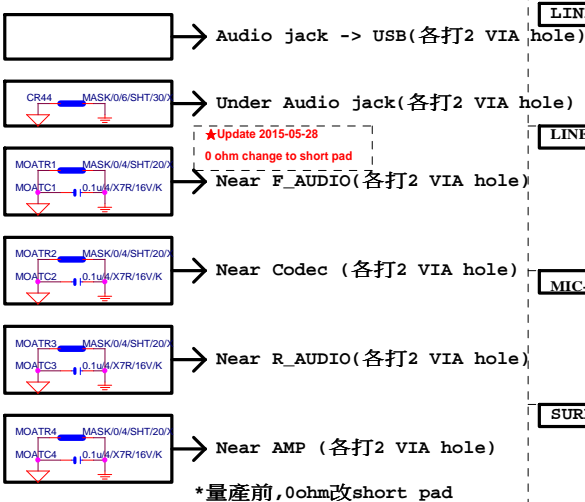
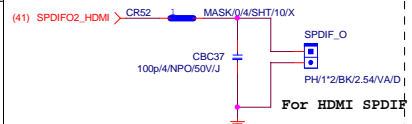
Gigabyte Technology			
Title			
KB_MS_USB3, R_USB30			
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
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2		1	

Rev 0.93

AZALIA JACK



SPDIF OUT



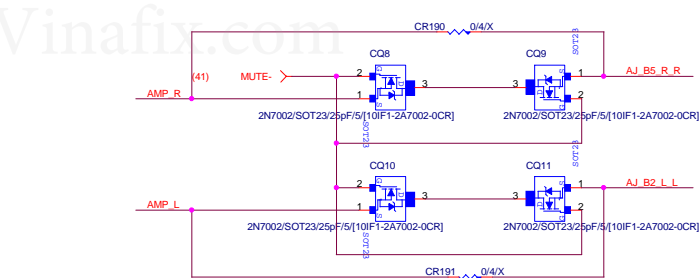
LINE-OUT

LINE-IN

MIC-IN

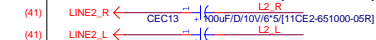
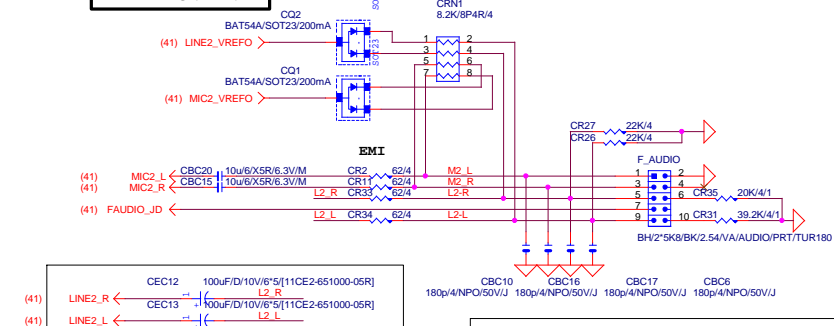
SURROUND

CEN/LFE



(45)

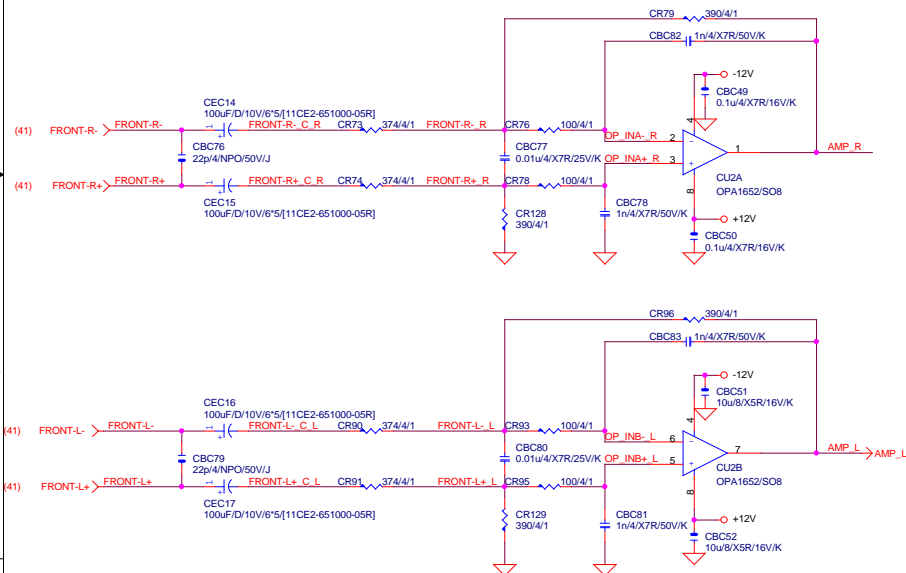
AZALIA FRONT PANEL



Gigabyte Technology

File	AUDIO JACK	
Size	Document Number	GA-Z170X-UD5
Custom	Rev	1.0
Date	Tuesday, July 14, 2015	Sheet 42 of 67

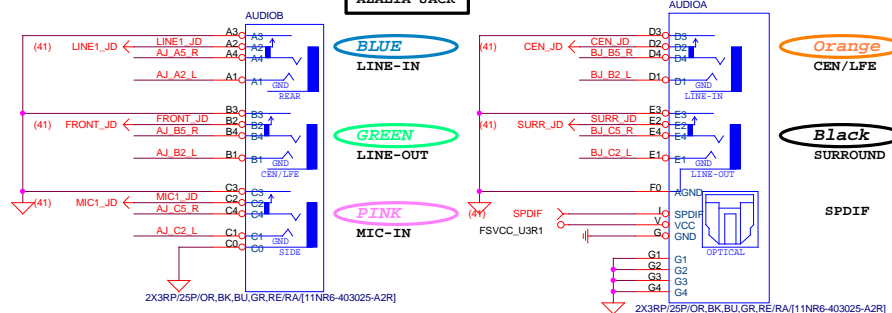
Differential to Single-End AMPLIFIED

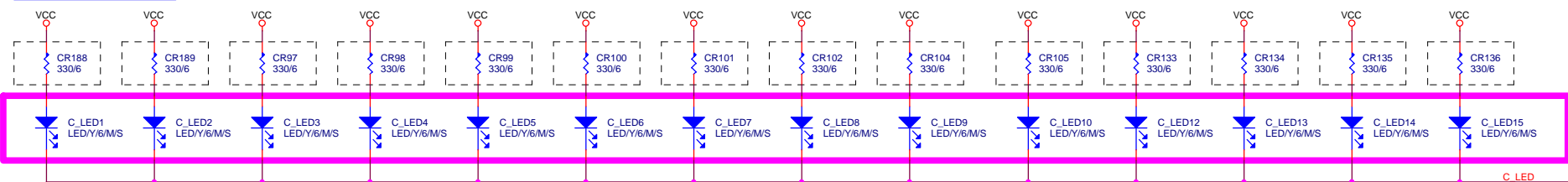


AZALIA JACK

BLUE
LINE-INGREEN
LINE-OUTPINK
MIC-INOrange
CEN/LFEBlack
SURROUND

SPDIF





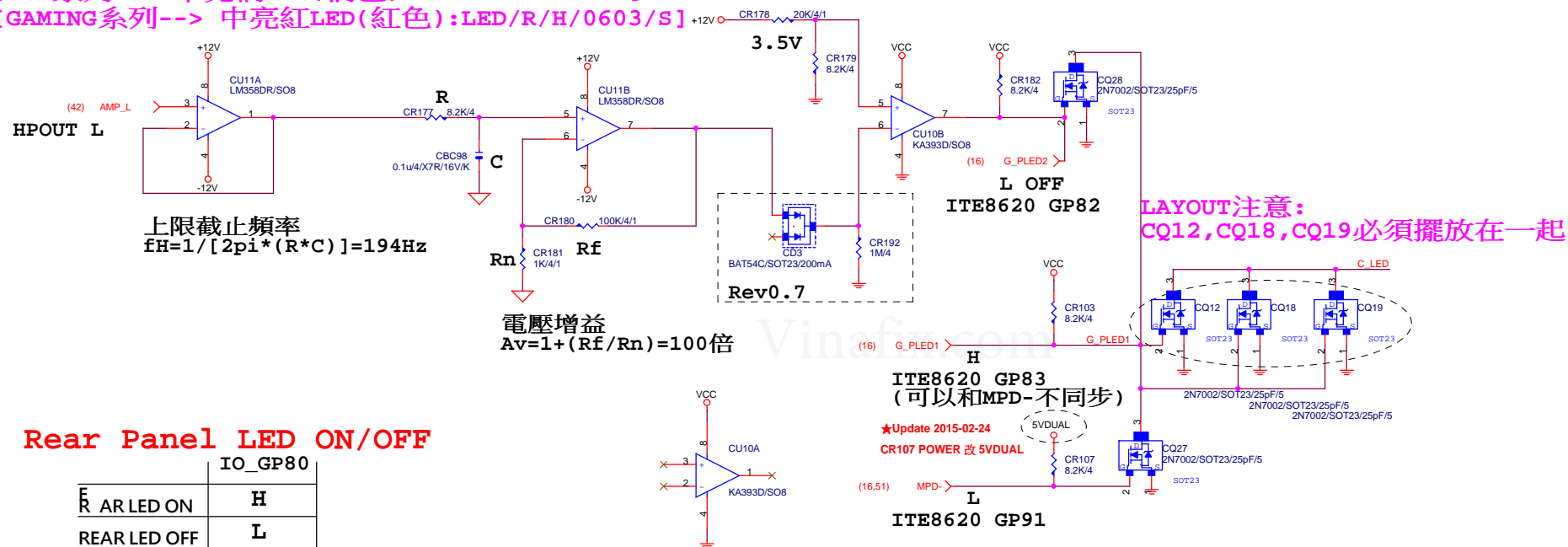
VALUE可變,LED顏色請自行修改

[UD系列--> 中亮黃LED(黃色):LED/Y/6/M/S]

[SOC系列--> 中亮橘LED(橘色):LED/O/M/0603/S]

[GAMING系列--> 中亮紅LED(紅色):LED/R/H/0603/S]

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Rear Panel LED ON/OFF

	IO_GP80
REAR LED ON	H
REAR LED OFF	L

CLOSE TO AUDIO JACK

ITE8620 GP80

LAYOUT OPTION : SOC/UD7系列要LAYOUT,
 其餘UD系列機種不留LAYOUT

AUDIO LED Control (沒有LPT model)

	IO_GP82	IO_GP83	IO_GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

AUDIO LED Control (有LPT model)

	IO_GP92	IO_GP17	IO_GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

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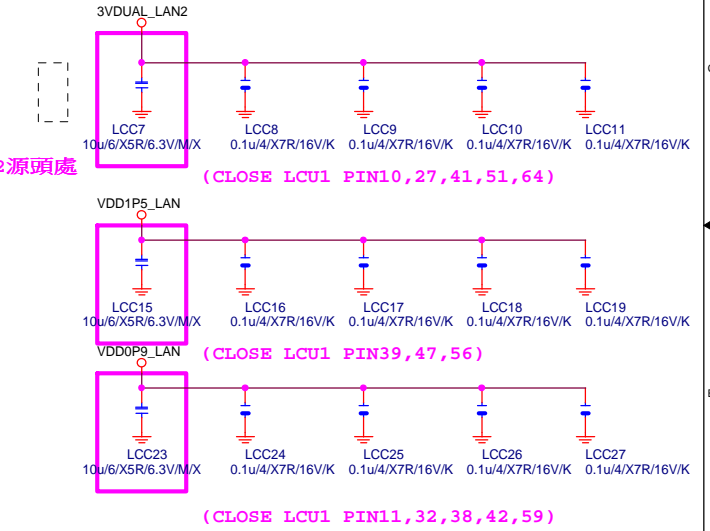
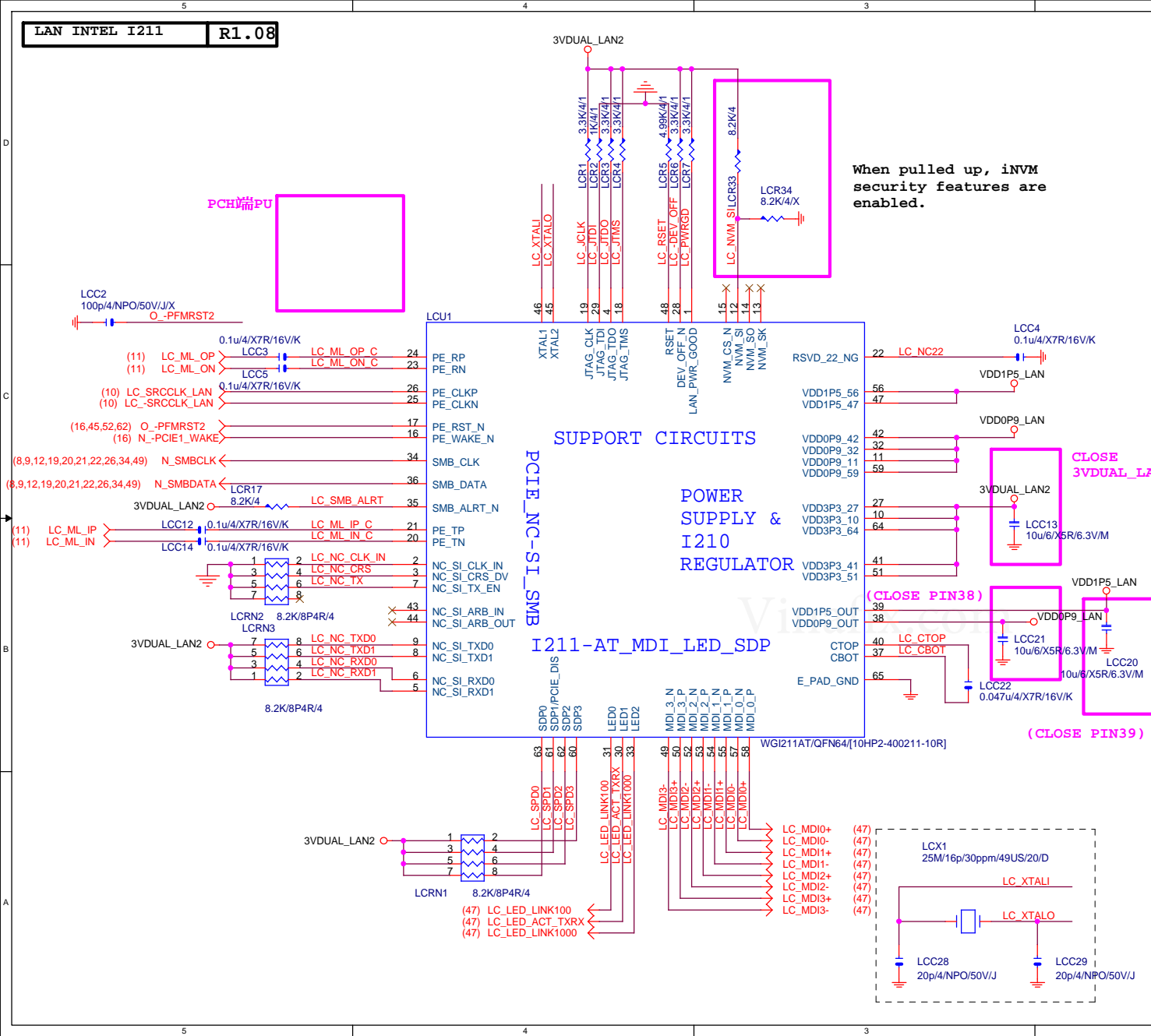
Title	AUDIO LED	
Size	Document Number	Rev
Custom	GA-Z170X-UD5	1.0
Date:	Tuesday, July 14, 2015	Sheet 43 of 67

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Title			ASM1142 USB3.1A		
Size	Document Number				Rev
Custom	GA-Z170X-UD5				1.0
Date:	Tuesday, July 14, 2015			Sheet 44 of 67	1

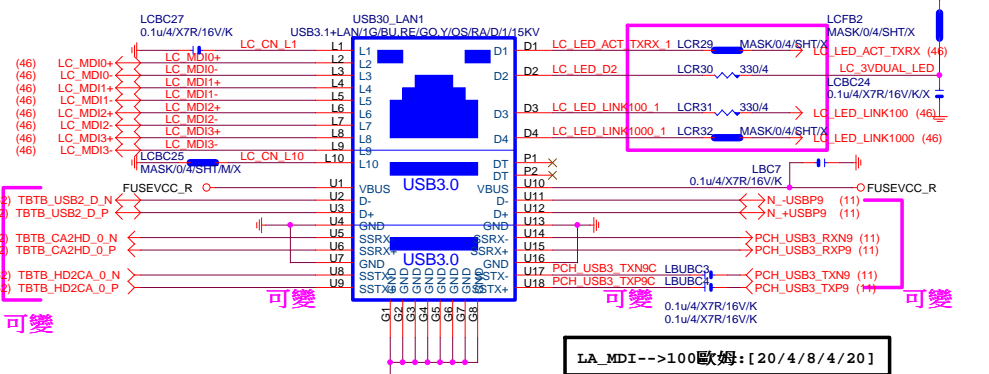
[illegible][illegible]



USB LAN CONNECTOR-B R1.08

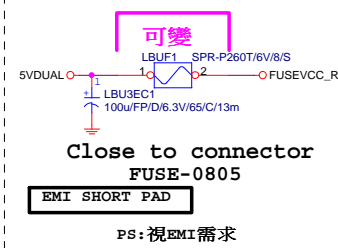
note:可變更USB NAME

[I211]

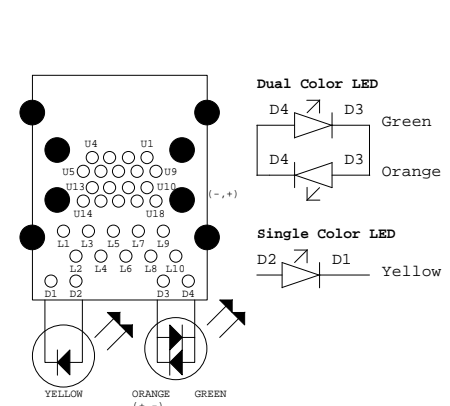


USB POWER

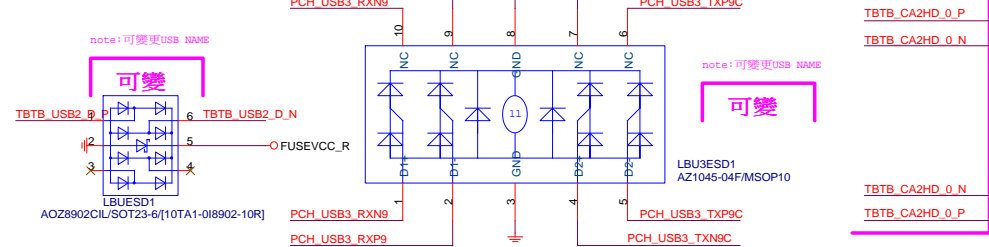
note:可變更FUSE



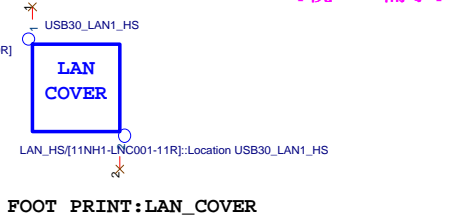
USB30 LAN LAYOUT示意图



RMA ESD PROTECT



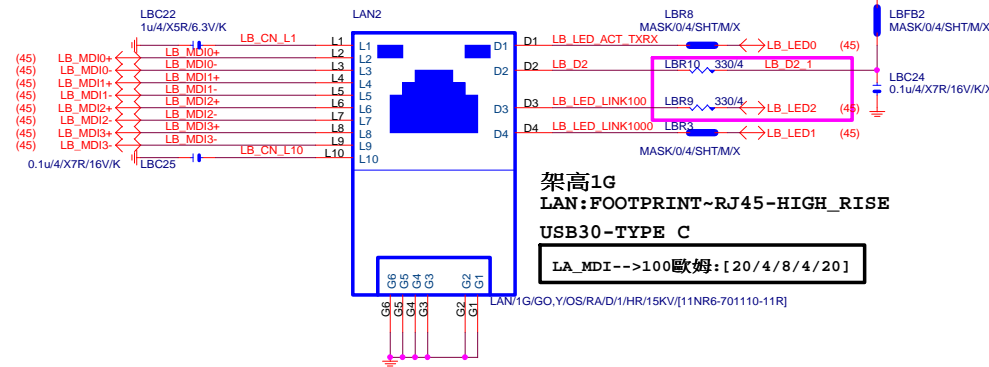
LAN COVER



USB LAN CONNECTOR-C

note:可變更USB NAME

[I211]



USB POWER

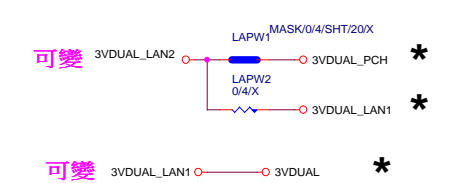


NOTE:

- 3VDUAL_LAN1,3VDUAL_LAN2 對接POWER供應電流 [目前暫接3VDUAL]
- USB2.0/3.0對應USB PORT [目前暫接USB 0,1,2,3 PORT]
- USB DROOP/DROP E-CAP
- USB OC線路

LAN POWER

note: lan power連接及電流



~USB30_LAN1設定在ERP可LAN WAKEUP

~USB30_LAN2由獨立LAN POWER L1117供給

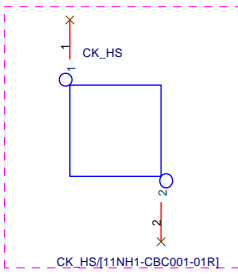
Gigabyte Technology			
LAN CONNECTOR-I219+I211			
Size	Document Number	Rev	1.0
Custom	GA-Z170X-UD5		
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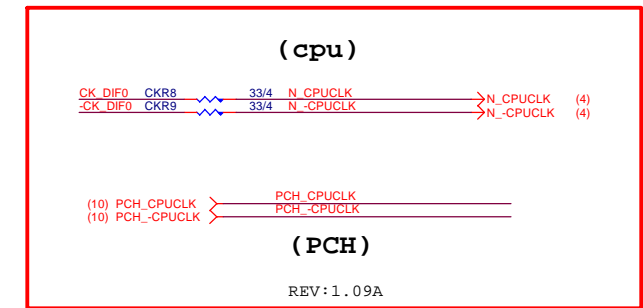
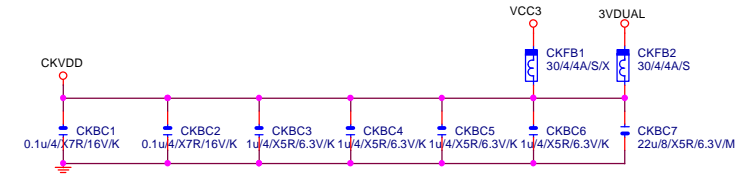
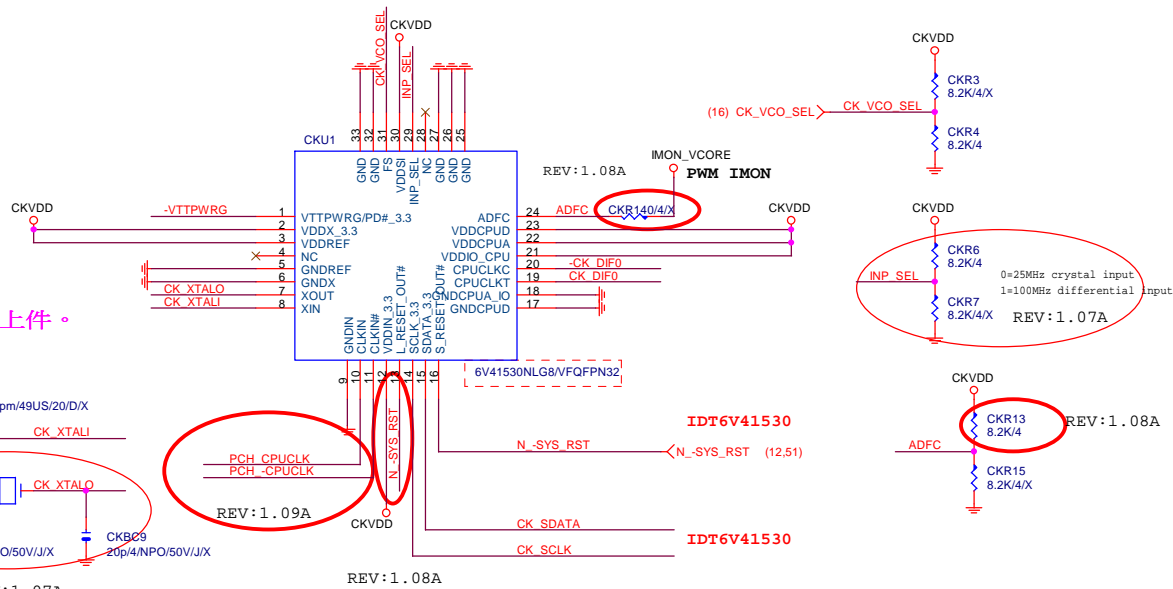
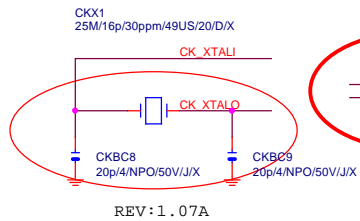
GIGABYTE™

Title			Etron EJ179V		
Size	Document Number				Rev
Custom	GA-Z170X-UD5				1.0
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IDT6V41530

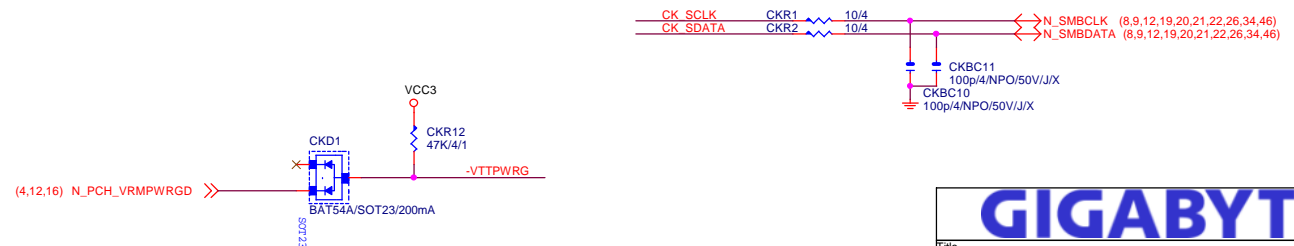


*可變，依需求上件不上件。



INP_SEL	Input
0	Crystal
1	CLK_INP/N

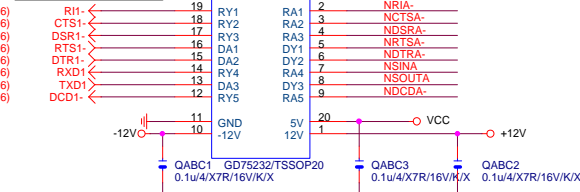
CK_VCO_SEL	VCO
0	400M
1	1200M

**GIGABYTE™**

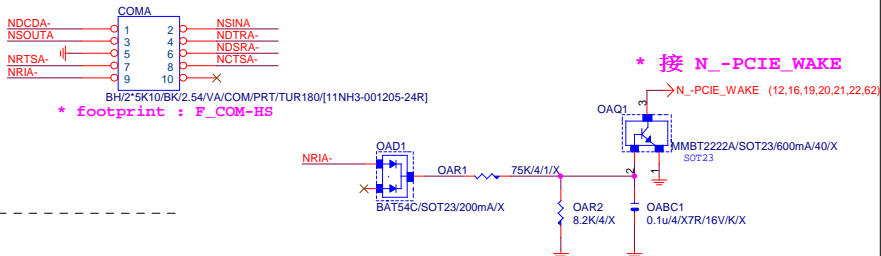
IDT6V41530_CLK BUFFER

Size Custom	Document Number GA-Z170X-UD5	Rev 1.0
Date:	Tuesday, July 14, 2015	Sheet 49 of 67

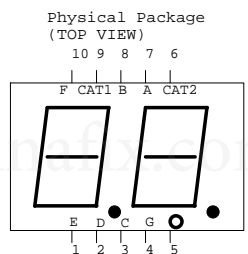
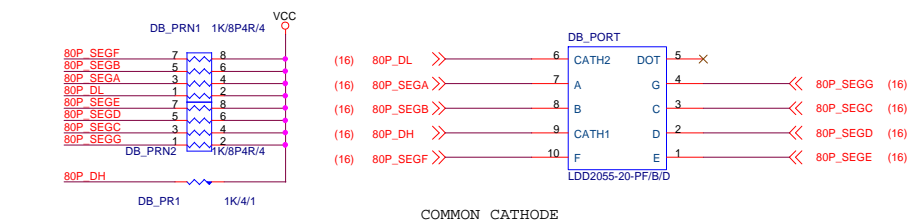
COM PORT



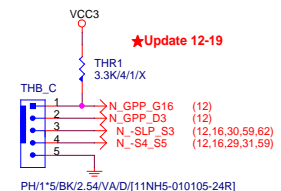
COMA



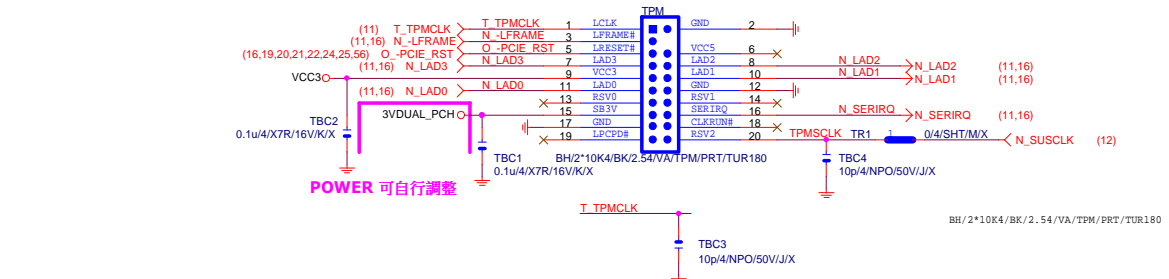
80 PORT



Thunderbolt

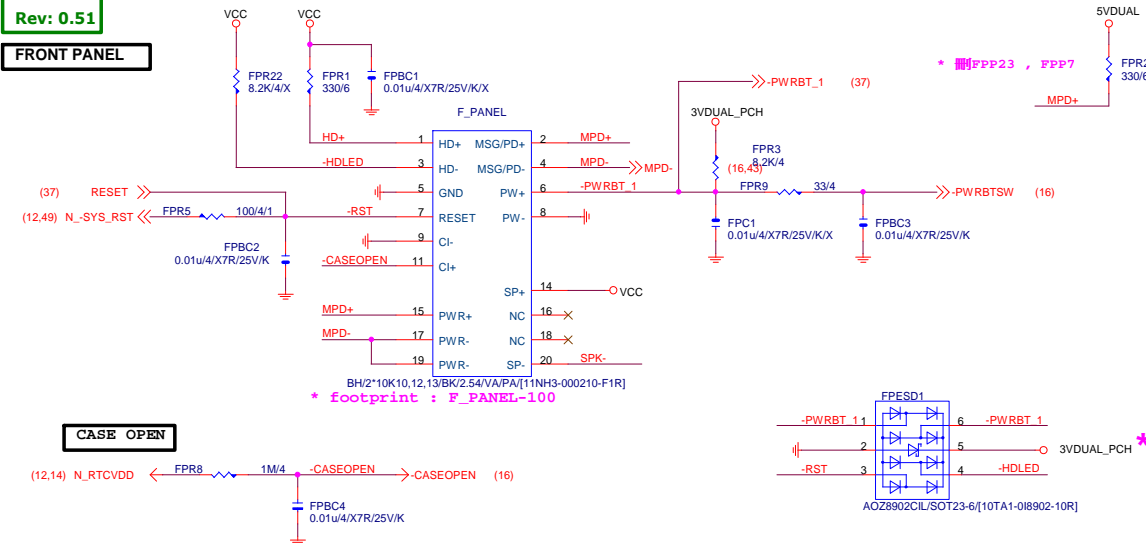


TPM CONNECT



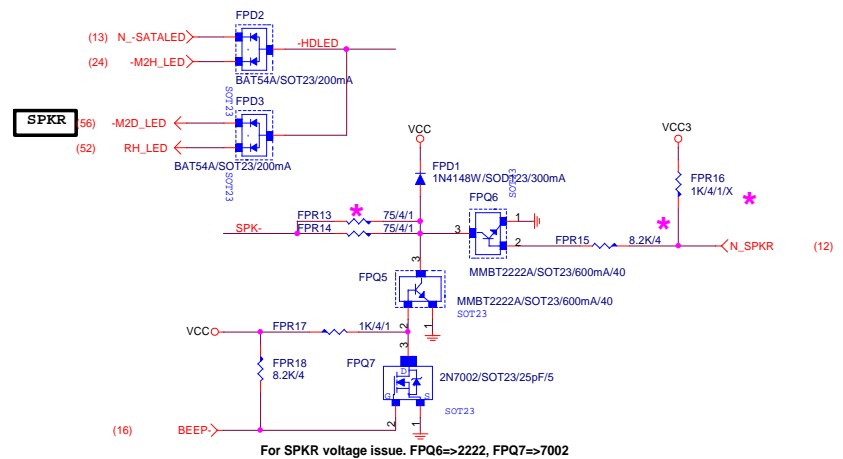
Rev: 0.51

FRONT PANEL



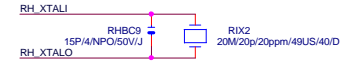
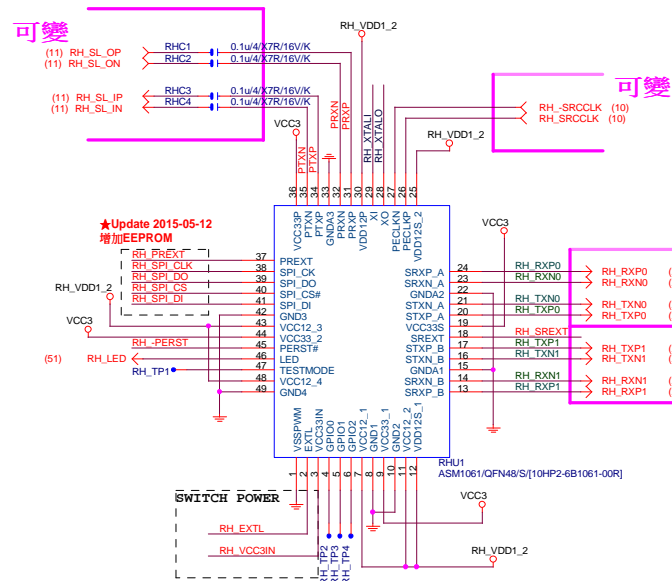
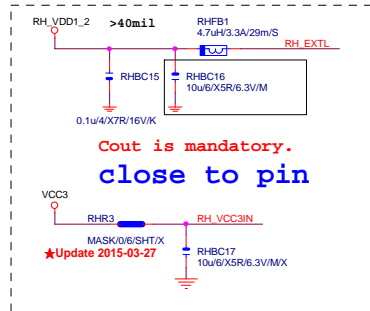
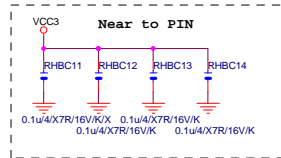
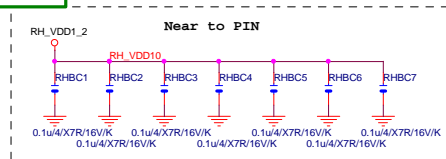
SATA LED SATALED# signal open-collector,pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3

SPKR



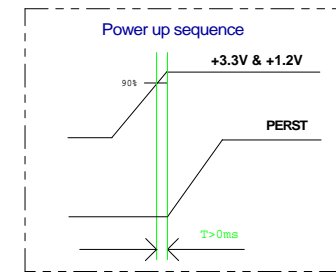
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Gigabyte Technology			
Title			
FRONT PANEL			
Size	Document Number	GA-Z170X-UD5	
Custom		Rev 1.0	
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SATA PORT 0

SATA PORT 1



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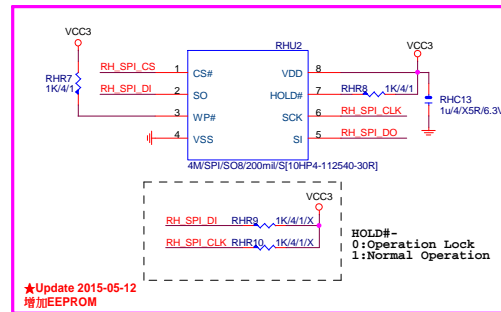
(驗證完畢可移除)

可變動

(16,45,46,62) O_PFMIRST2

★Update 2015-03-27
移除RH_VDD1_2 external power

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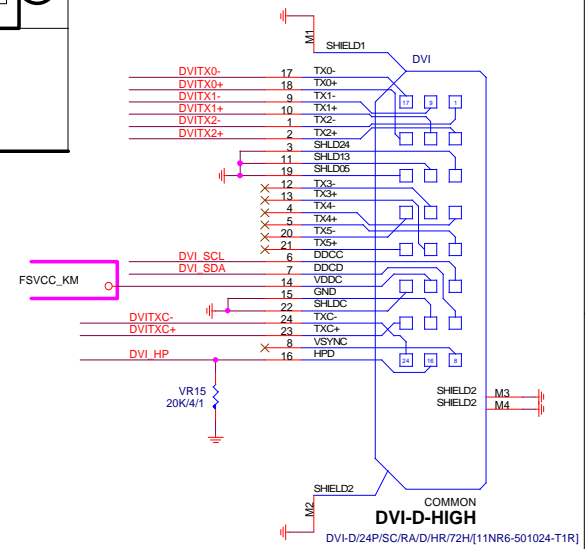
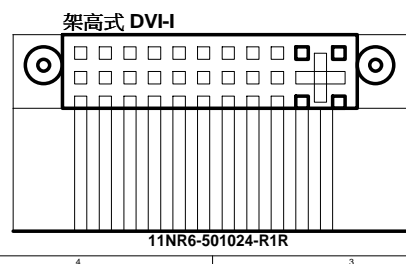
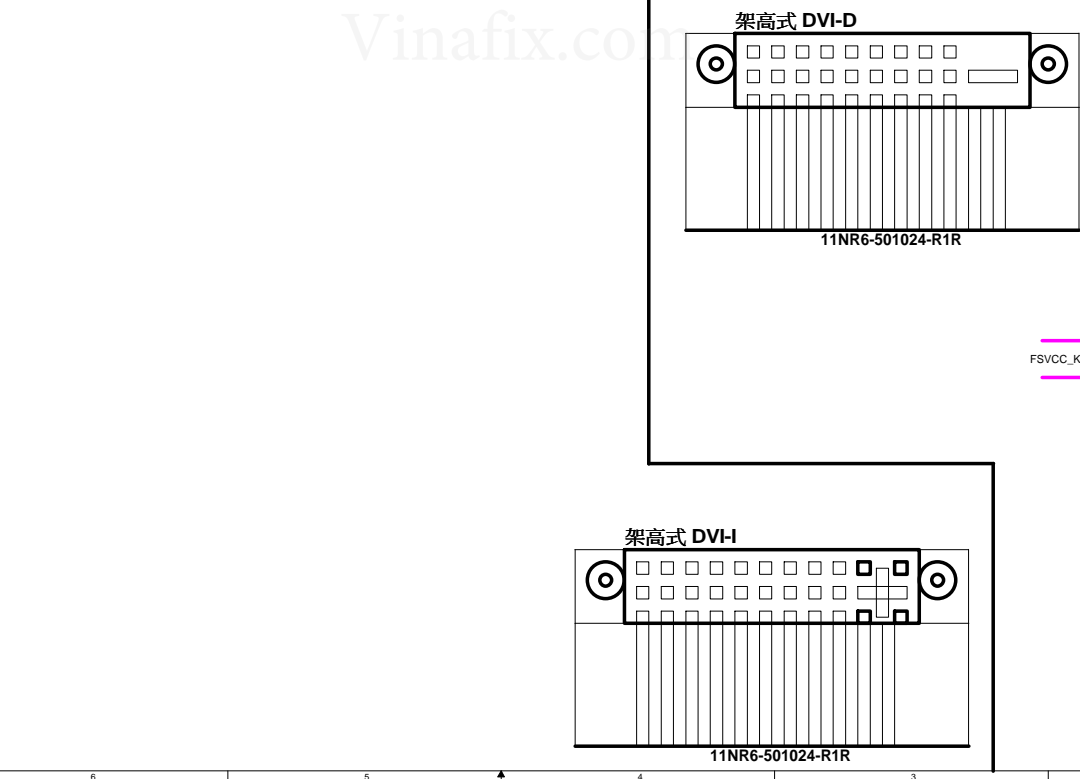
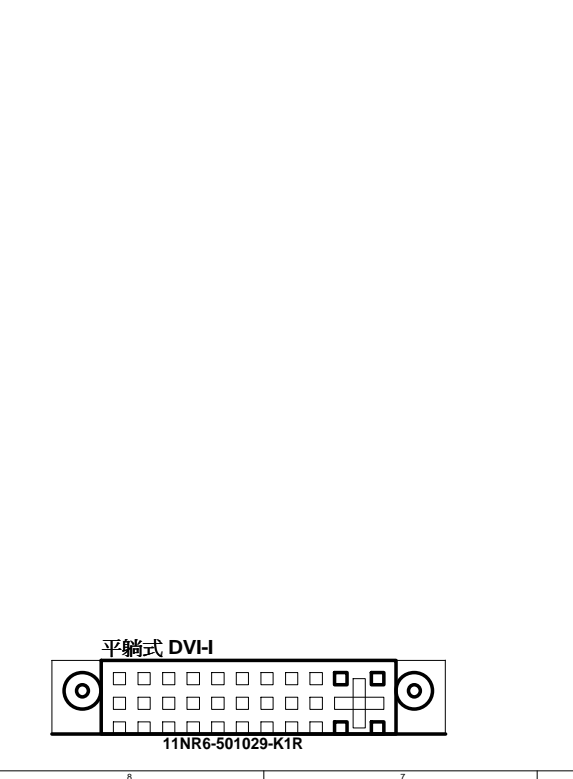
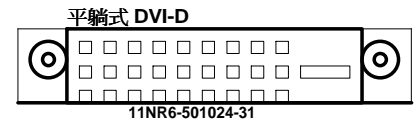
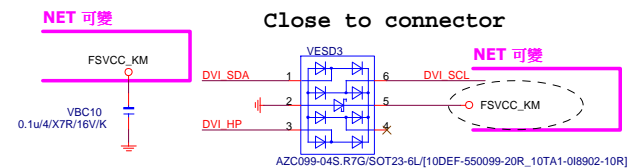
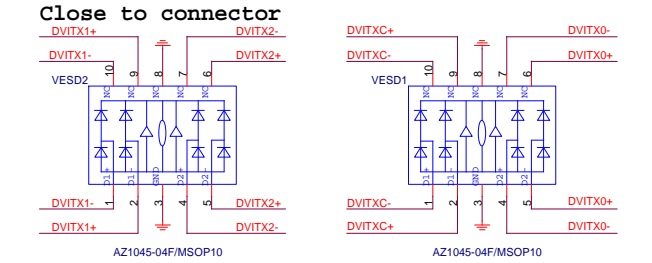
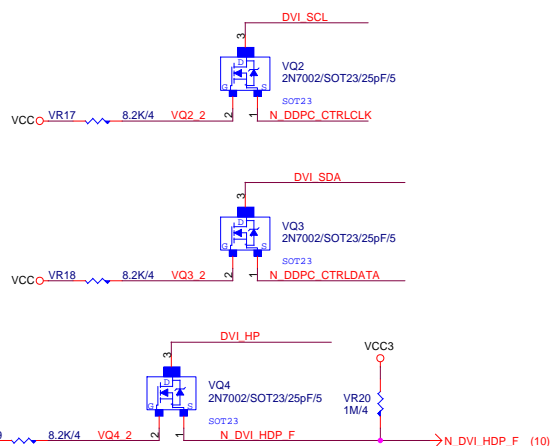
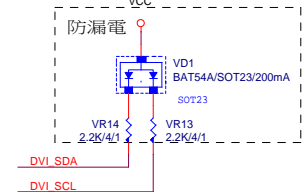
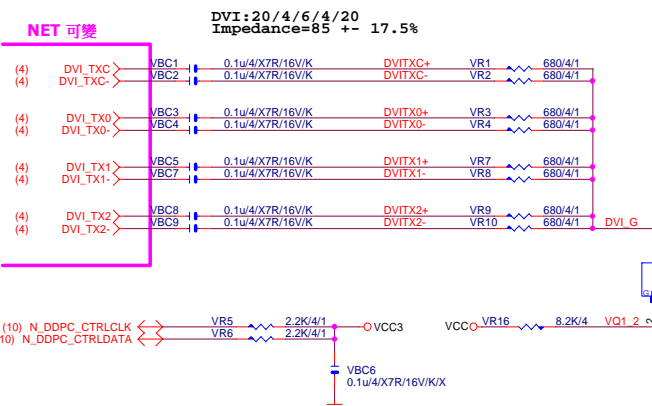


H/W Strapping

refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W

GIGABYTE™			
Title			
ASM1061			
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
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Gigabyte Technology			
Title			
HDMI20 MCDP2800-BA			
Size	Document Number		Rev
C	GA-Z170X-UD5		1.0
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M.2 Lane2 from PCH port19

(57) M2_PCIE_IN13 < 0.22u/4/X5R/6.3V/K M2DC15
(57) M2_PCIE_IP13 < 0.22u/4/X5R/6.3V/K M2DC16

M.2 Lane2 from PCH port20

(57) M2_PCIE_TN14 < 0.22u/4/X5R/6.3V/K M2DC9
(57) M2_PCIE_TP14 < 0.22u/4/X5R/6.3V/K M2DC10

M.2 Lane3 from PCH port21

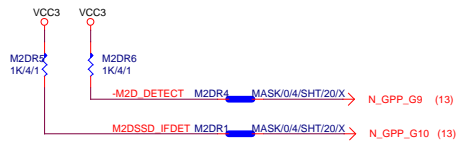
(57) M2_PCIE_IN15 < 0.22u/4/X5R/6.3V/K M2DC35
(57) M2_PCIE_IP15 < 0.22u/4/X5R/6.3V/K M2DC36

M.2 Lane4 from PCH port22

(57) M2_PCIE_IP16 < 0.22u/4/X5R/6.3V/K M2DC33
(57) M2_PCIE_TP16 < 0.22u/4/X5R/6.3V/K M2DC34

(10) CK_M2D_100M_DN
(10) CK_M2D_100M_DP
需與M2_-CLKREQ對應

支援SATA and M.2 function



M.2 有插卡 / 没插卡 GPP_G9	M.2插何種卡? GPP_G10	SATA Express 插何種硬碟? GPP_E0/E1/E2/F0	IO19 (S0)	IO20 (S1)	IO21 (S2)	IO22 (S3)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA	SATA	SATA	SATA (For M2)
		SATA Express (Low)	SATA	SATA	SATA	SATA (For M2)
	PCIe Mode (Hi)	SATA (Hi)	PCIEx4 (For M.2)			
		SATA Express (Low)	PCIEx4 (For M.2)			
没插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	SATA (S0)	SATA (S1)	SATA (S2)	SATA (S3)
		SATA Express (Low)	SATA Express (For S.E.0)		SATA Express (For S.E.1)	

M.2-SATA(S3)+SATA S0&S1&S2

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	H (SATA)	GPP_C21	H

M.2-SATA(S3)+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	L (S.E.)	GPP_C21	H

M.2X4

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	N/A	GPP_C21	H

M.2X2+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	L	GPP_C21	H

M.2X2+SATA S0&S1

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

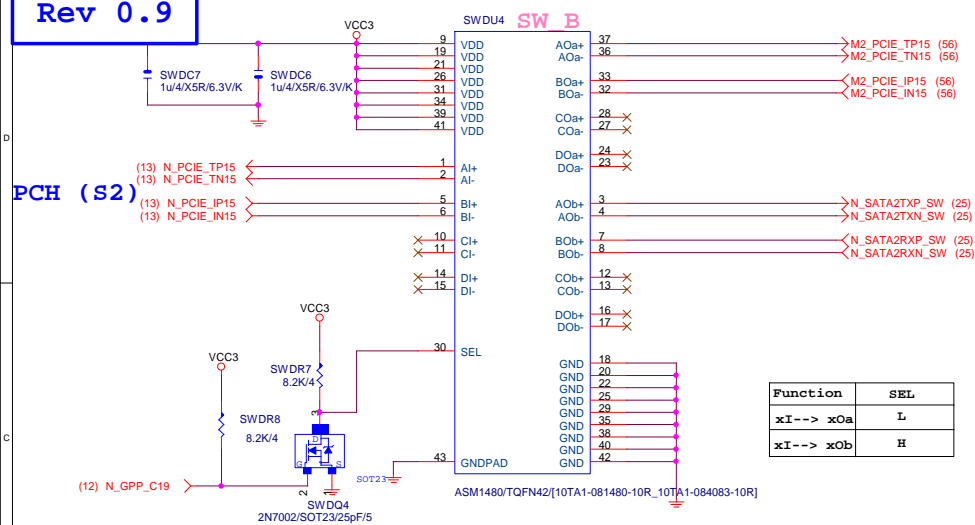
M.2沒插卡+SATA S0~S3

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	H	GPP_C21	L

M.2沒插卡+S.E.C&S.E.D

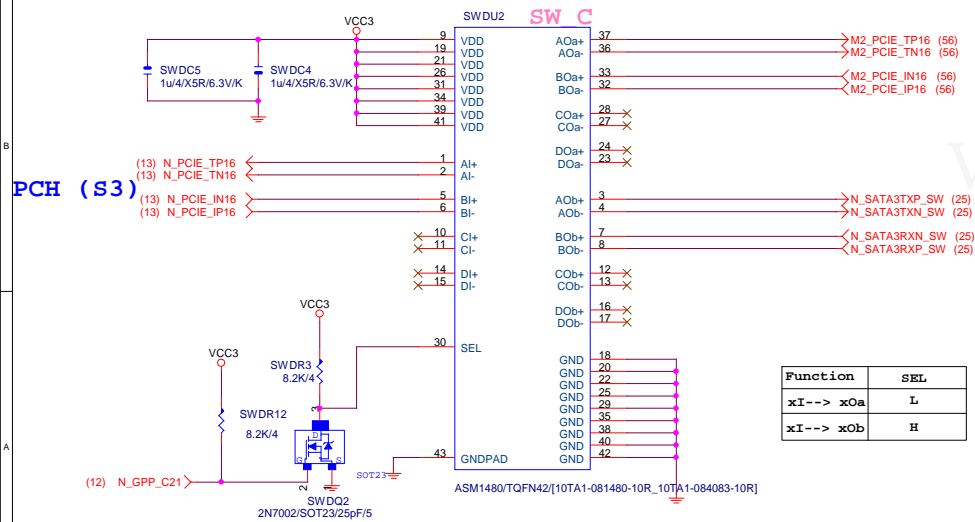
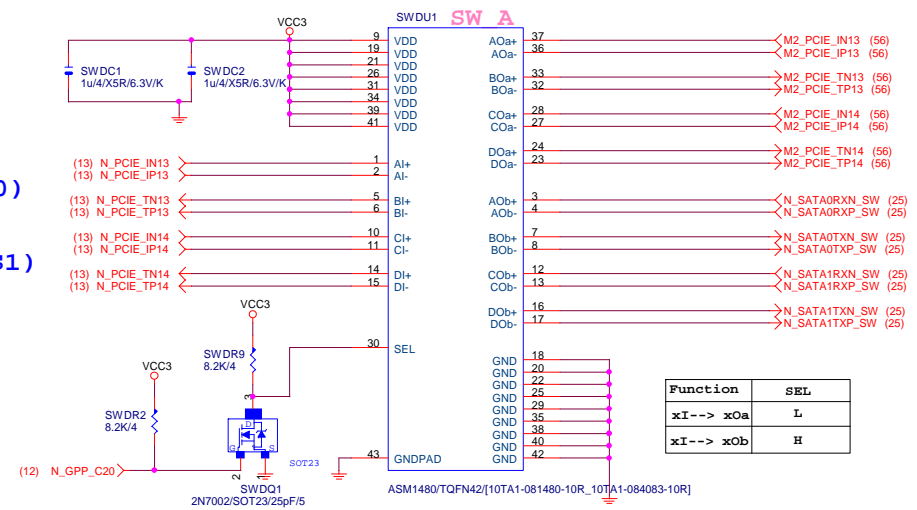
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	L	GPP_C21	L

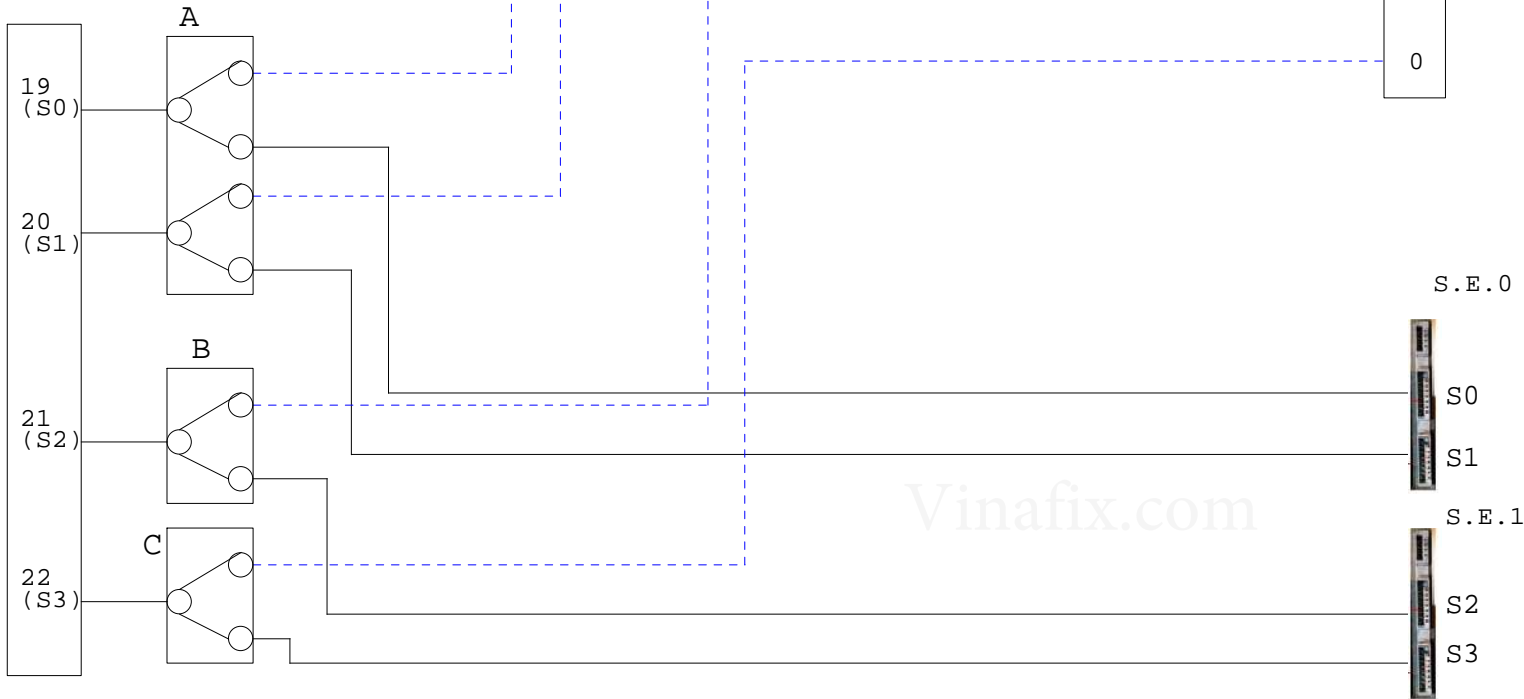
Gigabyte Technology			
Title	M.2 X4		
Size	Document Number	Rev	
Custom	GA-Z170X-UD5	1.0	
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PCH (S0)

PCH (S1)





3顆SW IC,

當使用M.2 (X2),
EXPRESS只可限定使用 S0&S1

ABC的切換方式:

下下下 : SE1+SE0

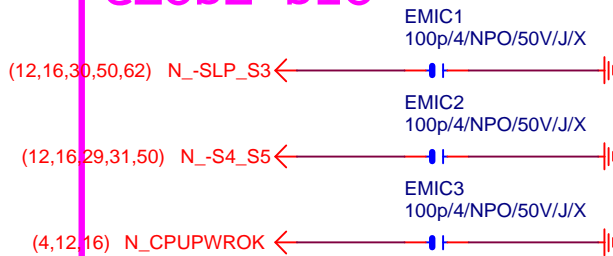
上上上 : M.2 X4

下上上 : M.2x2 + SE S0/S1

下下下上 : M.2 X1 + SE
S0/S1/S2

Title			
BLOCK DIAGRAM			
Size	Document Number		
Custom	GA-Z170X-UD5		
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	3	2	1

CLOSE SIO



CLOSE PCH



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GIGABYTE™

Title

EMI/ESD

Size
A

Document Number

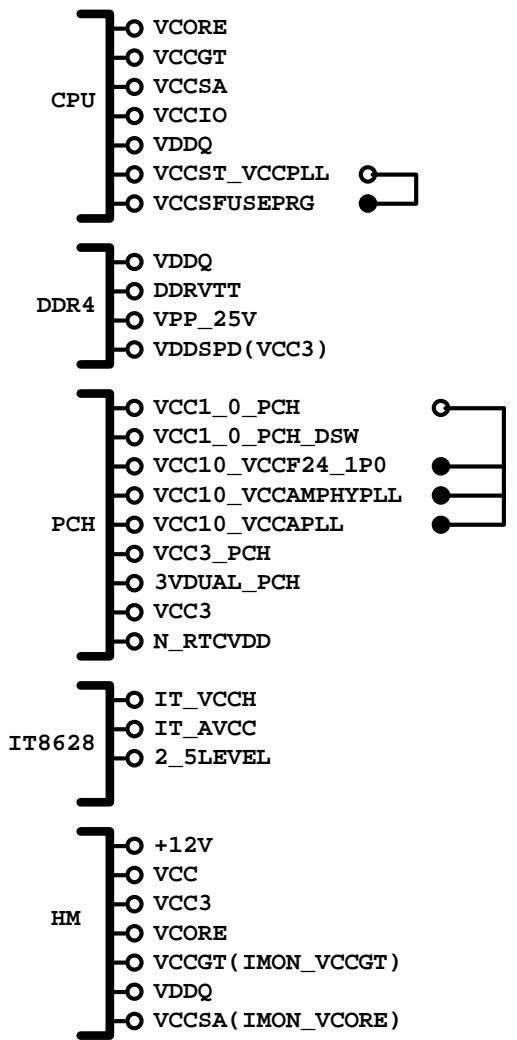
GA-Z170X-UD5

Rev
1.0

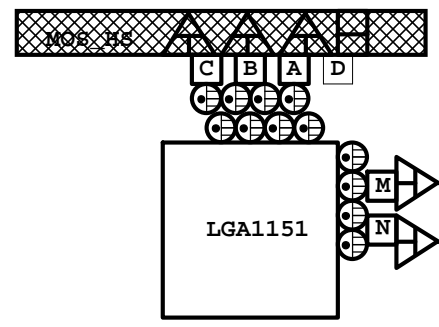
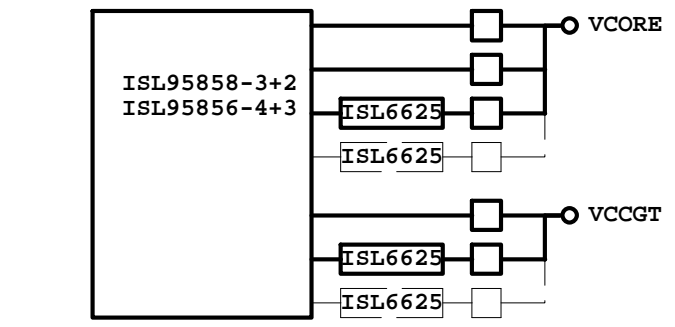
Date: Tuesday, July 14, 2015

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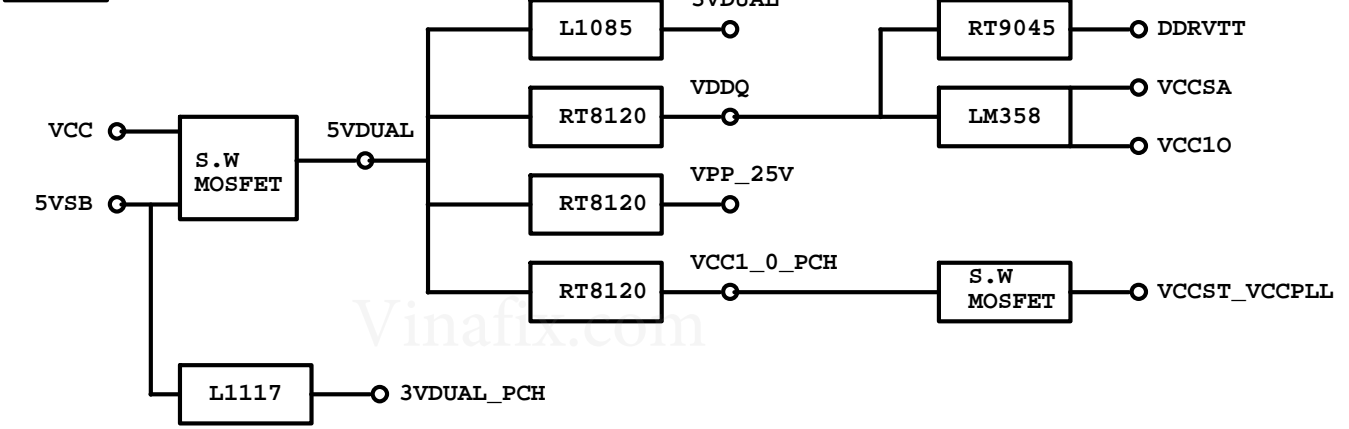
POWER BLOCK MAP



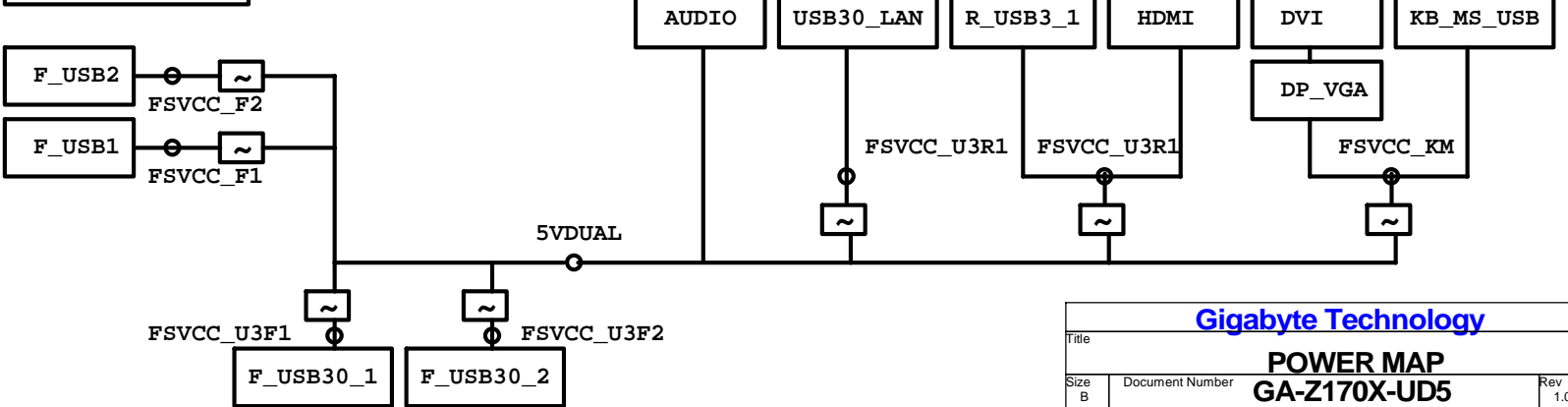
VCORE/VCCGT



POWER



FUSE POWER F/R



固態電容料號.請自行修改

日系黑色固態	Capture Value
11C02-C85600-01R	560u/FP/D/6.3V/68/C/8m
11C05-C82700-01R	270u/FP/D/16V/88/C/12m
11C05-C61000-01R	100u/OS/D/16V/66/C/30m
11C02-C51000-01R	100u/FP/D/6.3V/65/C/13m

日系一般固態	Capture Value
11C02-685600-01R	560u/FP/D/6.3V/68/8m
11C05-882700-01R	270u/FP/D/16V/88/12m
11C05-661000-03R	100u/OS/D/16V/66/30m
11C02-651000-02R	100u/OS/D/6.3V/66/30m

台系固態	Capture Value
11C02-661000-09R	100u/OS/D/6.3V/66/A/35m
11C05-691000-09R	100u/OS/D/16V/69/A/35m
11C05-8C2700-09R	270u/FP/D/16V/8C/A/10m
11C02-695600-09R	560u/FP/D/6.3V/69/A/11m

PWM料號

		料號	Capture Value	Footprint
PWM	ISL95856	10TA1-695856-01R		IC52QFN-6x6-G
PWM	ISL95858	10TA1-695858-01R		IC52QFN-6x6-G
PWM	IR35201	10TA1-635201-00R		IC56QFN-9VRS4339
PWM	IR3570	10TA1-603570-00R		IC40MLFP-ISL95835
PWM	RT8237C/D	10TA1-608237-01R		IC10DFN-NIS5132

REGULATOR

		料號	Capture Value	Footprint
	NCT3103S	10GL2-203103-01R	NCT3103S/SOP8/2A	IC8-EPSOIC

IRON CHOKE

	料號	Capture Value	SIZE	Footprint	
DIP	11LC5-M4500C-01R	0.5uH/40A/IMD109/M/D	10*10	CHOKE05U-40A-1PQ-3	閃電P
DIP	11LC5-M4500C-11R	0.5uH/40A/IMD109/M/NP/D	10*10	CHOKE05U-40A-1PQ-3	無閃電P
DIP	11LC5-M2500C-01R	0.5uH/20A/IMD0809/M/D	8*8	CHOKE1U-R50M-IF	


Skylake Iron Choke閃電P導入機種如下:
[1] Z170/H170 機種全部導入
[2] B150/H110Gaming機種導入,
其餘不導入

Ferrite

	料號	Capture Value	SIZE	Footprint
DIP	11LC5-F3500C-11R	0.5uH/32A/INCG109/FSI/D	10*10	CHOKE05U-40A-1PQ-3
DIP	11LC5-F2500C-11R	0.5uH/25A/INC0809/F/D	8*8	CHOKE1U-R50M-IF
SMD	10LC5-F4300C-01R	0.3uH/40A/SIUC/FR/S	10*7	CHOKE11X8MM-SMD

BEAD

	料號	Capture Value	SIZE	Footprint
DIP	10LFB-15470A-01R	47/4030/15A/S	4*3	BEADC8B-BPH_SMD



Title

RT8120_DDR4 POWER

Size

Document Number

Custom

GA-Z170X-UD5

Date:

Tuesday, July 14, 2015

Sheet

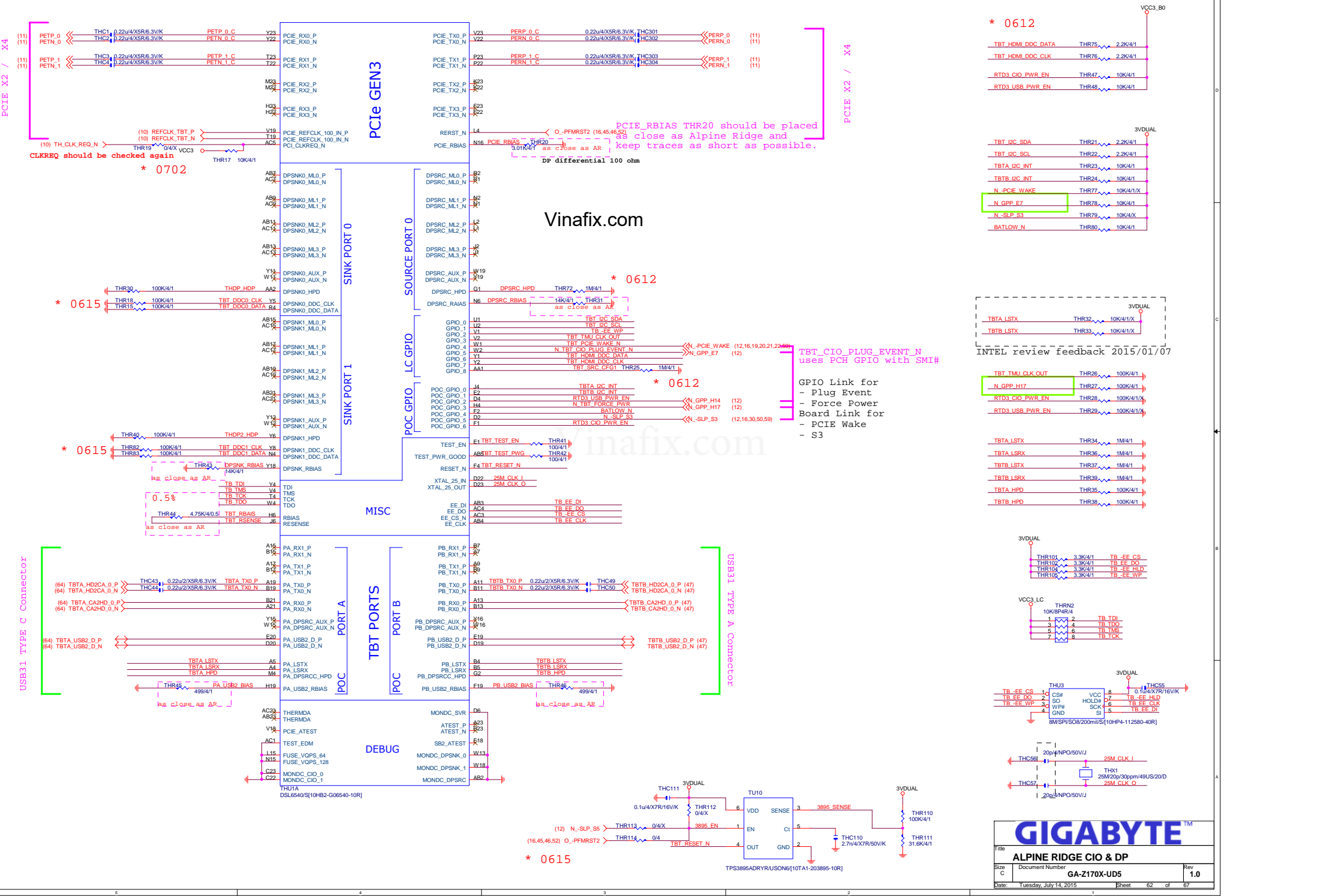
61

of

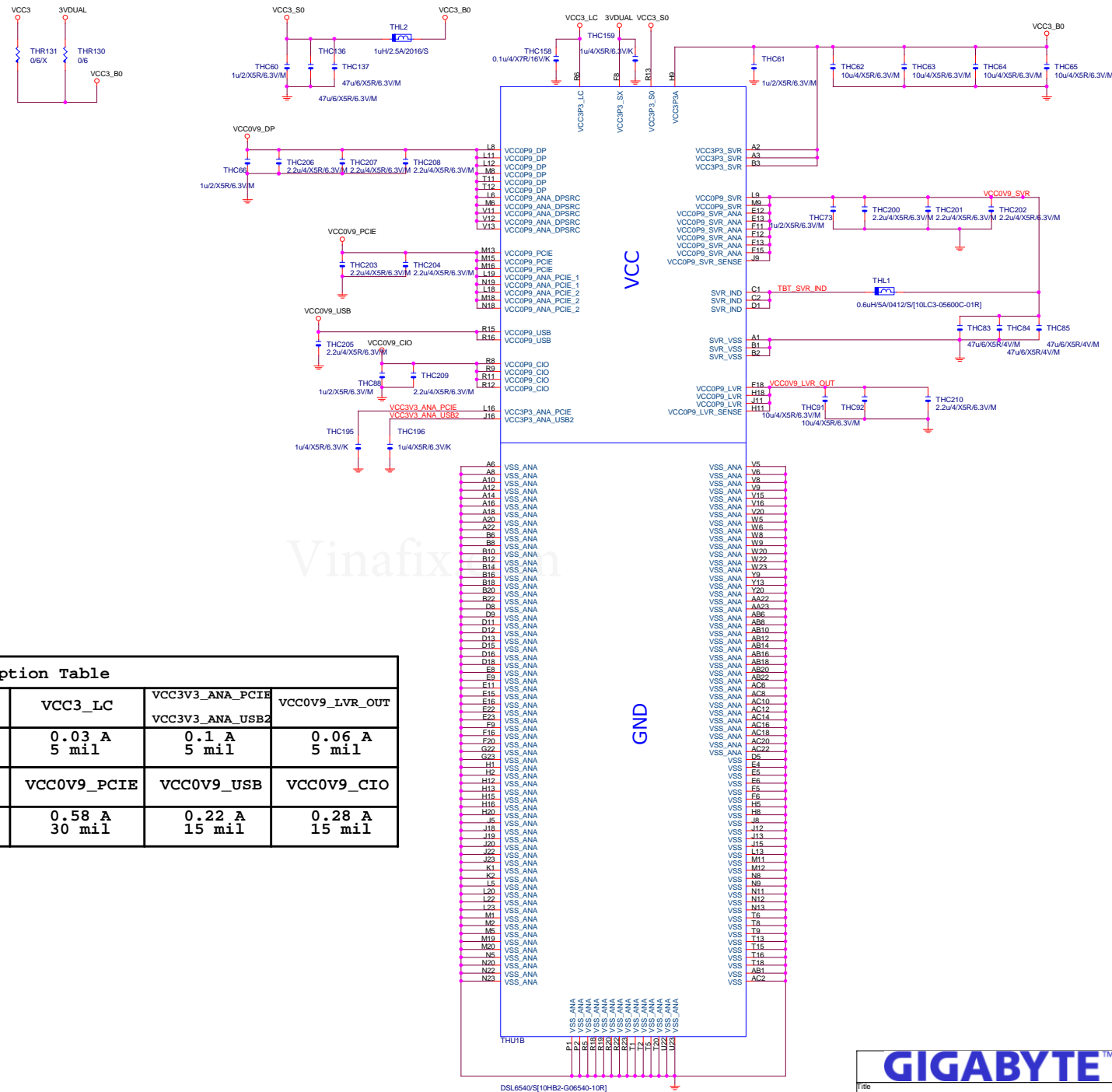
67

Rev

1.0



INTEL AR USB31 module SCH 0.61 (2015/06/15)



Power Consumption Table

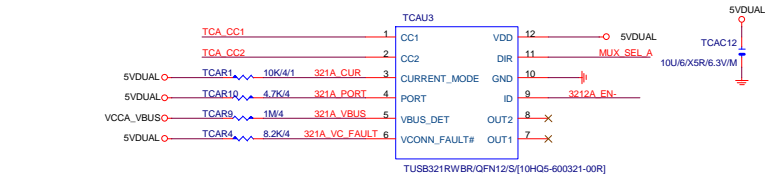
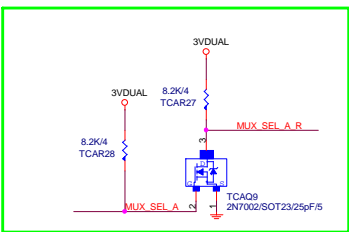
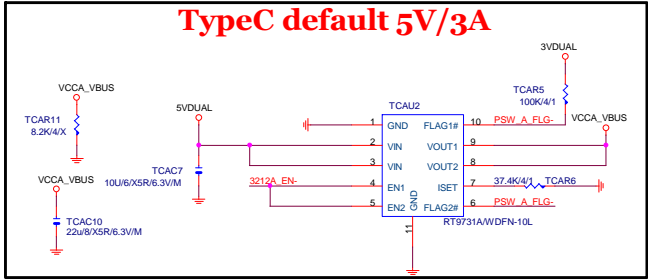
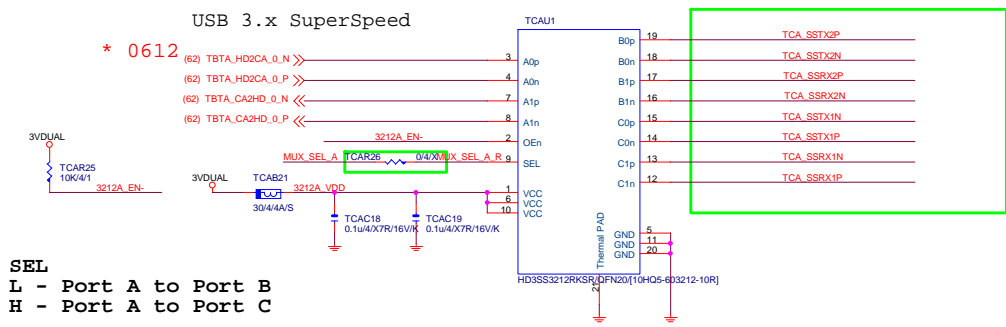
	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil

GIGABYTE

ALPINE RIDGE POWER

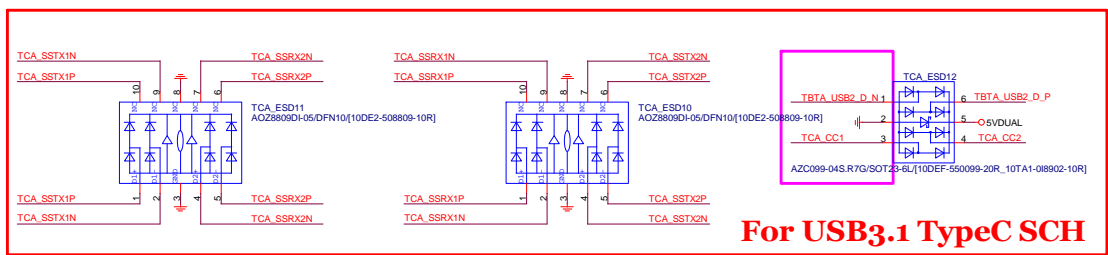
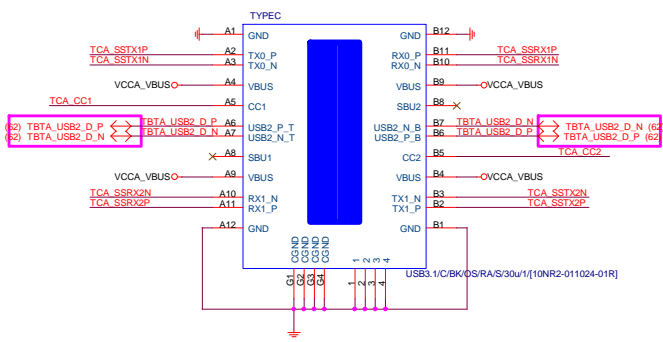
GA-Z170X-UD5
Rev 1.0
Date: Tuesday, July 14, 2015 Sheet 63 of 67

INTEL AR USB31 module SCH 0.61 (2015/06/15)



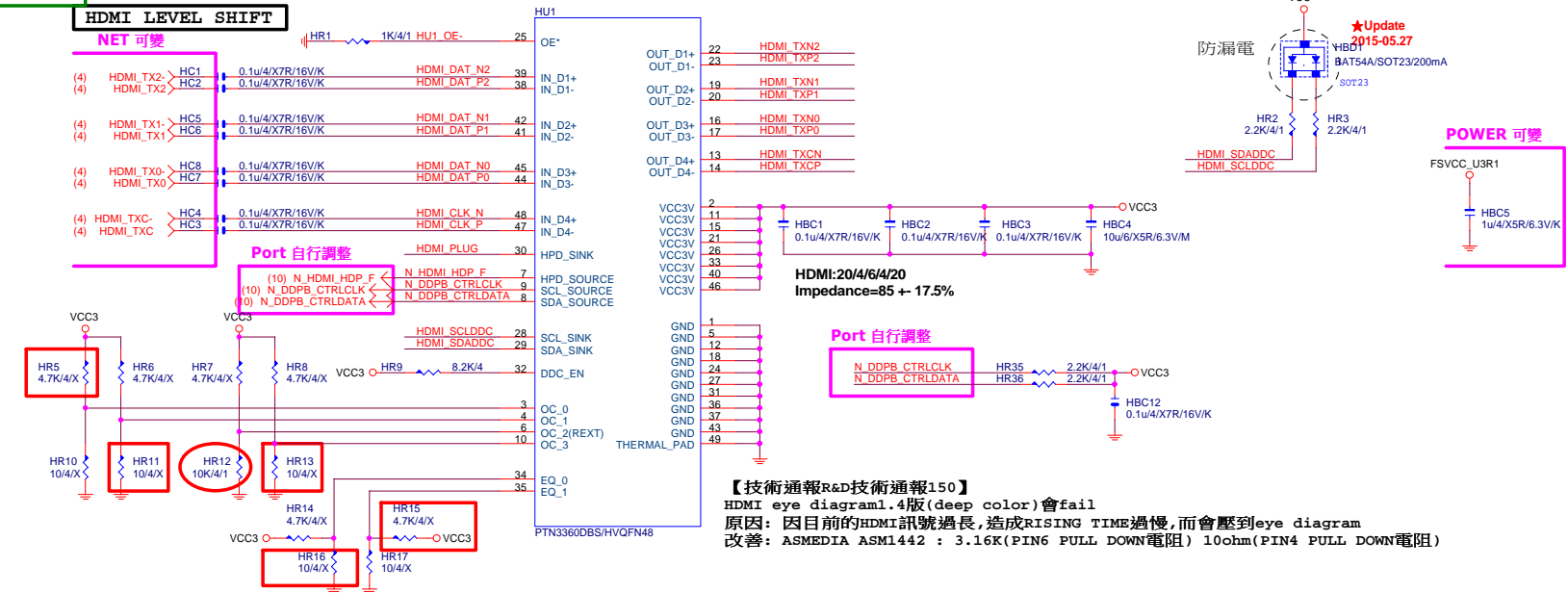
CURRENT MODE
L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

PORT
H - HOST
L - Device
NC - Dual Role

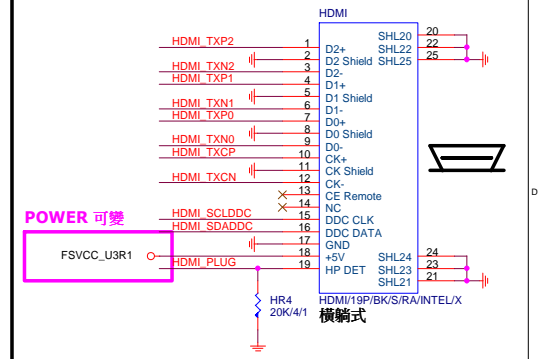


Color markers can be changed by model

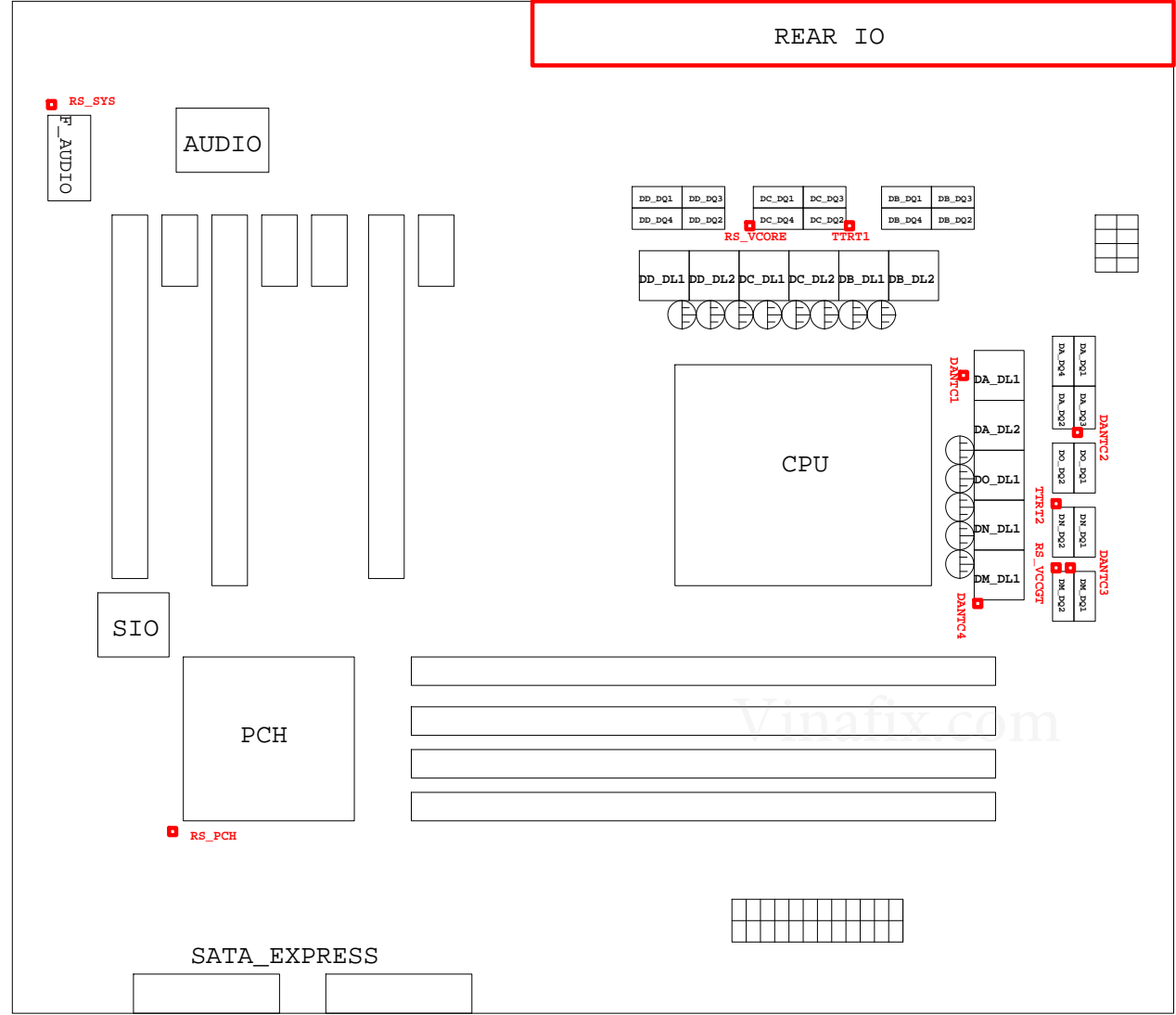
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Title		
TI TUSB321		
Size		
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PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K



直立式
P/N:11NR6-H01019-K1R



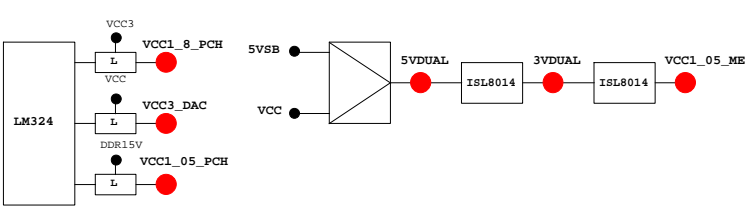
熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
RS_VCORE	DC_DQ4	N/A
RS_VCCGT	DM_DQ2	N/A
TTRT1	DC_DQ2	N/A
TTRT2	DN_DQ2	N/A
RS_PCH	PCH	N/A
RS_SYS	F_AUDIO	N/A

PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	PWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

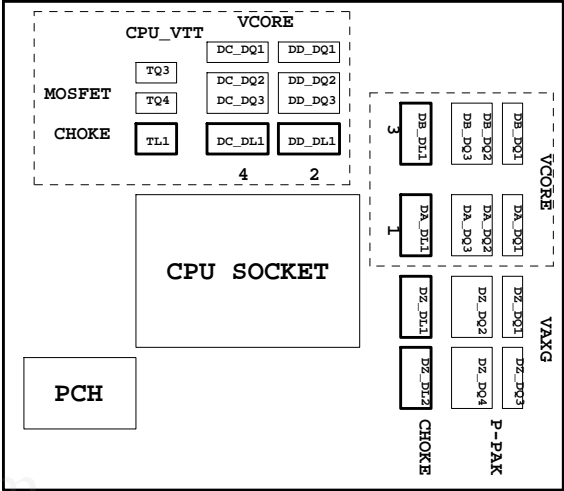
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCI_E_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/CLK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VBSBW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSW#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH